UNIVERSITY OF IOANNINA
SCHOOL OF SCIENCES
DEPARTMENT OF PHYSICS

Upgrade of the (barrel) muon trigger electronic system of the CMS experiment at CERN

Nikitas Loukas

PhD Thesis

IOANNINA 2018

ΠΑΝΕΠΙΣΤΗΜΙΟ ΙΩΑΝΝΙΝΩΝ
ΣΧΟΛΗ ΘΕΤΙΚΩΝ ΕΠΙΣΤΗΜΩΝ
ΤΜΗΜΑ ΦΥΣΙΚΗΣ

Αναβάθμιση του ηλεκτρονικού συστήματος σκανδαλισμού των μιονίων του πειράματος CMS στο CERN της Ελβετίας

Νικήτας Λούκας

ΔΙΔΑΚΤΟΡΙΚΗ ΔΙΑΤΡΙΒΗ

ΙΩΑΝΝΙΝΑ 2018

Three-member Advisory Committee

- Nikolaos Manthos, Associate Professor, Department of Physics, University of Ioannina, Greece (Thesis Supervisor)

- Konstantinos Fountas, Professor, Department of Physics, University of Ioannina, Greece (Head of High-Energy Physics LABoratory, HEPLAB)

- Ioannis Papadopoulos, Assistant Professor, Department of Physics, University of Ioannina, Greece

Seven-member Assessment Committee

- Ioannis Evangelou, Associate Professor, Department of Physics, University of Ioannina, Greece

- Konstantinos Fountas, Professor, Department of Physics, University of Ioannina, Greece (Head of High-Energy Physics LABoratory, HEPLAB)

- Panagiotis Kokkas, Professor, Department of Physics, University of Ioannina, Greece (Head of the Physics Department)

- Dimitrios Loukas, Director of Research at National Centre of Scientific Research (NCSR) "Demokritos", Greece

- Nikolaos Manthos, Associate Professor, Department of Physics, University of Ioannina, Greece (Thesis Supervisor)

- Ioannis Papadopoulos, Assistant Professor, Department of Physics, University of Ioannina, Greece

- Ioannis Strologas, Assistant Professor, Department of Physics, University of Ioannina, Greece

Ancient Greeks noticed that amber attract small objects when rubbed with fur. Along with lightning, this phenomenon is one of humanity's earliest recorded experiences with electricity. Both electric and electricity are derived from the Latin electrum, which came from the Greek word for amber (ilektron).

In quantum mechanics, the behavior of an electron in an atom is described by an orbital, which is a probability distribution rather than an orbit.

Uncertainty principle declares that for any given instant of time, the position and momentum of an electron cannot both be exactly determined, and that a state where one of them has a definite value corresponds to a superposition of many states for the other.

To my Ilektra and her mother Lydia.
To my parents.

Η έγκριση της διδακτορικής διατριβής από το τμήμα Φυσικής του Πανεπιστημίου Ιωαννίνων δεν υποδηλώνει αποδοχή των γνωμών του συγγραφέα. (Ν.5343/1932, άρθρο 202, παρ. 2)

Acknowledgments

Starting from the Ioannina group, I would like to thank all the members of High-Energy Physics Laboratory (HEPLAB) and especially my supervisor Nikos Manthos who has guide me from my first steps as a graduate student. I would like also to thank the head of HEPLAB, Prof. Costas Fountas for getting me involved in the CMS L1 upgrade and for being my mentor. I also thank Ioannis Papadopoulos for teaching me the secrets of the Unix environment and George Sidiropoulos for supporting me in my first VHDL steps. I thank my colleagues and friends, Giannis Flouris and Vangelis Paradas, with whom I worked closely on the validation of the BMTF algorithm and the control of the system during commissioning. I also thank the Emeritus Professor and former head of HEPLAB, Frixos Triantis for encouraging me during the PhD.

I would like to thank the CMS muon trigger group and especially Karol Bunkowski for sharing their knowledge and experience and my good friend Andrea Triossi with whom I worked closely during BMTF commissiong. Also I thank my colleagues of the HEPHY group, Janos Ero, Dinyar Rabady and Claudia Wulz. Especially Janos Ero who transmitted me his knowledge of the legacy muon track finders. I gratefully thank Greg Iles, Andrew Rose, Alessandro Thea and all the UK-CMS trigger group for their support in the use of the MP7 card which is the heart of the BMTF system.

Last, but not least, I would like to mention the five-months period I spent as an Erasmus student in 2013, working on the new TCDS card FC7 in the EP-ESE-BE group at CERN. Despite the fact that I didn't work entirely for my thesis, this period was essential for the experience and knowledge I gained on firmware development and on optical links. This period proved to be critical for my PhD and for that reason I would like to thank the head of the Back-End (BE) section of the Experimental Physics Department − Electronic Systems for Experiments group (EP−ESE), Francois Vasey for giving me this opportunity and Paschalis Vichoudis for supervising me.

Abstract

The CMS experiment is one of the most well-known experiments in the world and one of the four operating in the Large Hadron Collider (LHC) where hadron bunches are accelerating and colliding up to a nominal energy of 14 TeV. The CMS consists of detector layers where electrical signals are generated by: particle hits, energy adsorptions and tube ionizations. Those signals are collected by electronic Front-End (FE) boards, which transform the signals to digital information. This information is processed by a complex electronic and subsequent computing network in order to reconstruct the particle information (electrons, photons, muons and jets), produced after hadron collisions in the center of CMS. Then physicists from all over the world collaborate and perform data analysis and search for new Physics phenomena that are consistent with the data collected in the CMS experiment.

The CMS Level-1 Trigger system (L1T) selects useful physics events at a rate of 100 KHz having an input rate of 40 MHz. Initially, the system was designed to operate to a luminosity of $10^{34}\text{cm}^{-2}s^{-1}$. According to the LHC phase I schedule, on 2016 the luminosity has been increased by a factor of two and reached $5\text{x}10^{34}\text{cm}^{-2}s^{-1}$ with the LHC phase II upgrade in 2025. The phase-I upgrade of the L1T system is completed in 2016 and provides the required hardware with state of the art Field-Programmable Gate Arrays (FPGAs) to compensate with the requested performance for the higher luminosity environment the next years. The L1T has two main branches: The calorimeter trigger and the muon trigger.

The upgraded muon trigger system is divided in three pseudorapidity (η) regions that follow the physical structure of the CMS: the barrel, the endcap and the common overlap regions. The Endcap Muon Track Finder (EMTF) has replaced the old Cathode Strip Chamber Track Finder (CSCTF) in the $1.24 < |\eta| < 2.4$ region. The Overlap Muon Track Finder (OMTF) covers the region with $0.83 < |\eta| < 1.24$ and has replaced both CSCTF and the Drift Tube Track Finder (DTTF), in that region. The Barrel Muon Track Finder (BMTF) covers the $|\eta| < 0.83$ and has replaced the older DTTF running until the end of 2015.

The phase-I upgrade of the barrel muon trigger is presented in this Thesis. Multiple Track Finders (TFs), running in the legacy system, in several hardware cards, integrated to twelve high-end processor boards. In the BMTF each Master Processor virtex-7 (MP7) board processes data and finds muon tracks within one wedge of muon detectors. The BMTF system is based on the μTCA standard replacing the old VME of the DTTF. The introduction of high-speed serial links running at 10 Gb/s, reduced the interconnections and made the system easier for any future intervention.

The BMTF, described in Chapter 4, finds muon tracks from data primitives generated in the barrel of CMS. The data are concentrated from the new upgraded sector collector system called TwinMux. The TwinMux combines data derived from gas ionization (Drift Tube detectors, DT) and data derived from muon hits (Resistive Plate Chambers detectors, RPC) moving the architecture from a muon detector-based scheme (DT and RPC) to a geometry-based system (the barrel). The TwinMux applies a timing correction of the DT data-primitives as the RPC data-primitives "hits" carry less information but better time accuracy. In the barrel, the TwinMux systems fan-outs its results called "super-primitives" to the BMTF system. The transverse momentum p_T assignment unit of the BMTF has been improved by adding one extra logic branch to the assignment block (Subsection 4.1.2.3). The implemented algorithm in the BMTF has been validated by detailed studies and comparisons between the results of the BMTF hardware and a bit-by-bit software emulator. The upgrade of the barrel muon trigger have reduced the trigger rate for a similar efficiency to the DTTF, in order for the BMTF to operate under higher luminosity, until the phase-II trigger upgrade starting on 2023.

The chosen FPGA used in the BMTF provides a large number for hardware components. One third of the available hardware resources are utilized. The unused components are available for future algorithm improvements. The BMTF sends the "triggered" muon data to the next stage of the trigger chain called the micro Global Muon Trigger (μGMT). The μGMT receives also data from the Overlap and Endcap Muon Track Finders and sorts out the found muon tracks according to a predefined quality rank.

During the first quarter of 2016, the BMTF subsystem was integrated and commissioned in CMS underground cavern USC55. At this stage, several adjustments and replacements was carried out to ensure stability and reliability. At the end of the commissioning the BMTF was operated normally as a part of the new phase-1 upgrade of the Level-1 Trigger at CMS. In addition to BMTF, firmware for other subsystems of the Level-1 Trigger in CMS was developed. Logic based on sheared MP7 Hardware description Language (HDL) code, was implemented in three different subsystems: TwinMux, CPPF and AMC502 (AMC502 is part of the micro Global Trigger, μGT). These basic logic designs were used as infrastructure with which colleagues from the respectively groups developed their designs.

Finally, during the preparation years of the CMS trigger upgrade, work has been done for the Timing and Control Distribution System (TCDS) upgrade. In a short time of this period, three FPGA Mezzanine Cards (FMCs) was evaluated versus a reference commercial card. The evaluation proved that the cards were able to run optical links at the nominal data bandwidth which varies between them (0.4 Gb/s to 10 Gb/s). These FMCs are used in the TCDS carrier card, designed at CERN, called Flexible Card kintex-7 (FC7).

The work described on this Thesis, carried out according to the Technical Design Report: TDR2013 [1]. Four papers concerning the BMTF system, have been published, after work was presented in different conferences: TWEEP2015 [2], TWEEP2016 [3], ICHEP2016 [4] , VCI2016 [5]. One Detector Note [6] and one Twiki web-page [7] with useful instructions for the BMTF user have also been provided by the Thesis's writer.

Contents

List of abbreviations

ADC	Analog-to-Digital Converter
ALGO	Implemented ALGOrithm
ALICE	A Large Ion Collider Experiment
AMC	Advanced Mezzanine Card
AMC13	Single width AMC - Serves TCDS functions on BE systems in CMS
AMC502	Commercial double width AMC - Vadatech
APD	Avalanche Photo Diodes
ARM	Advanced RISC Machine
ASIC	Application Specific Integrated Circuit
ATCA	Advanced Telecommunications Computing Architecture
ATLAS	A Toroidal LHC ApparatuS
BANK	On Xilinx FPGAs, BANK is a group of I/O pins that share a common resources
BC0	Bunch Crossing Zero - First Bunch Crossing of the orbit
BE	Back-End
BER	Bit-Error Rate
BERT	BER Test
BGo	TCDS commands that control the system (start, stop, resync ...)
BMTF	Barrel Muon Track Finder
BPIX	Barrel region of PIXel detector
BRAM	FPGA's build-in Block RAM
BTI	Bunch and Track Identifier
BUF	FPGA buffer
BX	Bunch Crossing

CaloL1 The 1st Layer of the Calorimeter trigger

CaloL2 The 2nd Layer of the Calorimeter trigger

CB magnet Coil in the Barrel

CCC CERN Control Center

CERN European Laboratory for Particle Physics (Conseil Européen pour la Recherche Nucléaire)

CML Current Mode Logic

CMS Compact Muon Solenoid

CMT Clock Management Tile

CPLD Complex Programmable Logic Devices

CPM Central Partition Manager

CPPF Concentration Pre-Processing and Fan-out

CPU Central Processing Unit

CRC Cyclic Redundancy Check

CSC Cathode Strip Chamber

CSCTF CSC Track Finder

CTP7 Calorimeter Trigger Processor-Virtex7

DAQ Data AcQuisition

DAS DAQ System

DC/DC Direct Current to Direct Current converter

DDR3 Double Data Rate type three SDRAM

DEE Divided half EE

DQM Data Quality Monitoring

DRAM Dynamic Random-Access Memory

DSP Digital Signal Processor

DT Drift Tube

DTTF Drift Tube Track Finder

EB Barrel portion of ECAL covering pseudorapidity below 1.5

ECAL Electromagnetic CALorimeter

EE	Endcap portion of ECAL covering pseudorapidity between 1.6 and 3
EMTF	Endcap Muon Track Finder
ETTF	ETA Track Finder
EW	ElectroWeak
FC7	Flexible Card-Kintex7
FE	Front-End
FED	Front End Driver
FIFO	First-In First-Out memory
FINOR	FINal OR signal of partial trigger gives the Level-1 Accept
FMC	FPGA Mezzanine Card
FPGA	Field-Programmable Gate Array
FPIX	Forward region of PIXel detector
FSM	Finite State Machine
GbE	Gigabit Ethernet computer networking
GCT	Global Calorimeter Trigger
GMT	Global Muon Trigger
GOL	Gigabit Optical Link protocol
GRID	Global computer farm
GT	Global Trigger
GTH	Xilinx 7-series GTH transceiver
GTX	Xilinx 7-series GTX transceiver
GUI	Graphical User Interface
HB	Barrel portion of HCAL covering pseudorapidity less than 1.3
HCAL	Hadronic CALorimeter
HDL	Hardware Description Language
HE	Endcap portion of HCAL covering pseudorapidity between 1.3 and 3
HEP	High-Energy Physics
HEPHY	The Institute of High Energy Physics - Austrian Academy of Sciences (Institut für Hochenergiephysik - Österreichischen Akademie der Wissenschaften)

HEPLAB High-Energy Physics Laboratory, University of Ioannina

HF Very Forward portion of HCAL covering pseudorapidity between 3 and 5

HLT High Level Trigger

HO Outer Barrel Calorimeter (Hadronic)

HPC High Pin Count

HPD Hybrid PhotoDiode

HTRG High-quality TRiGger

I^{2}C Inter-Integrated Circuit

iBERT Xilinx IP (intellectual property) - integrated BERT

ICHEP International Conference on High Energy Physics

IEEE Institute of Electrical and Electronics Engineers

ILA Indegraded Logic Analyser

IP Internet Protocol

IPbus An IP-UDP interface that access FPGAs though 1 GbE

IPMI Intelligent Platform Management Interface

ISERDES Standard pin DESerializers

JINST Journal of Instrumentation

JTAG Joint Test Action Group; test and diagnostic bus standard by IEEE1149.x

L1A Level-1 Accept

L1T Level-1 Trigger

LC Lucent or Little or Local Connector. Type that interconnects two fiber channels

LEMO Connector named from engineer **Lé**on **Mo**uttet - Canton du Vaud, Switzerland

LHC Large Hadron Collider

LHCb Large Hadron Collider beauty experiment studding b-physics

LHCf Large Hadron Collider forward experiment

LINAC2 LINear ACcelerator

LPM Local Partition Manager

LSB Least Significant Bit

LTRG Low quality TRiGger

LUT Look Up Table

LVDS Low Voltage Differential Signaling

LVTTL Low Voltage TTL signals operate at 3.3-volt power supply

MAC Media Access Control

MB Muon Barrel station. When MB#, # indicates the number of station

ME Muon Endcap station. When ME#, # indicates the number of station

MC Drift tube MiniCrate

MCH MicroTCA Carrier Hub

MGT Multi-Gigabit Transceiver. Data-rate from 1 Gb/s to 56 Gb/s

MMC Module Management Controller

MMCM Mixed-Mode Clock Manager (similar to PLL)

MoEDAL Monopole and Exotics Detector At the LHC

MP7 Master Proccesor virtex-7

MSB Most Significant Bit

MTF6 Modular Track Finder virtex-6

MTF7 Modular Track Finder virtex-7

MTP MTP a brand of MPO interface connector. When MTP-#, # indicates the number of fiber channels

MUX multiplexer: device that selects one of several input signals as output

NIM Nuclear Instrumentation Module

OMTF Overlap Muon Track Finder

oRM optical Receiver Mezzanine

oRSC optical Regional Summary Card

OS Operating System

OSERDES Standard pin SERializers

oSLB optical Synchronization and Link Board

PACT PAttern Comparator Trigger

PATT data PATTern generator

PC Personal Computer

PCB Printed Circuit Board

PHTF PHi Track Finder

PI Partition Interface

PLL Phase Locked Loop

PRBS Pseudo-Random Binary Sequence

PS Proton Synchrotron

PSB Proton Synchrotron Booster

PU Pile-Up

QCD Quantum ChromoDynamics

QED Quantum ElectroDynamics

QUAD FPGA BANK that hosts 4 Multi-Gigabit Transceivers

RAM Random Access Memory

RARP Reverse Address Resolution Protocol

RCT Regional Calorimeter Trigger

RISC Reduced Instruction Set Computer

RISC Reduced Instruction Set Computing

RLDRAM Reduced Latency DRAM

ROB ReadOut Board

ROM Read Only Memories

ROS Read Out Server

RPC Resistive Plate Chambers

RTL Resistor-Transistor Logic

RX Receiver

SB Server Board

SC Sector Collector

SDRAM Synchronous Dynamic Random-Access Memory

SERDES FPGA's SERializers/DESerializers

SFP	Small Form-factor Pluggable transceiver
SLB	Synchronisation and Link Board
SM	Standard Model
SMA	SubMiniature version A - semi-precision coaxial RF connectors
SPI	Serial Peripheral Interface
SPS	Super Proton Synchrotron
SRAM	Static Random Access Memory
ST	muon detector STation
SWATCH	SoftWare for Automating conTrol Common Hardware
TCDS	Timing and Control Distribution System
Tcl	Tool command language
TCP	Transmission Control Protocol (over Internet Protocol)
TCS	Trigger Control System
TDR	Technical Design Report
TEC	Tracker (silicon strip detector) outer EndCap
TF	Track Finder
TIB	Tracker (silicon strip detector) Inner Barrel
TID	Tracker (silicon strip detector) Inner enDcap
TK	inner silicon TracKer
TMT	Time Multiplexing Trigger
TOB	Tracker (silicon strip detector) Outer Barrel
TOTEM	TOTal cross section, Elastic scattering and diffraction dissociation Measurement at the LHC
TP	Trigger Primitive
TPG	Trigger Primitive Generator
TRB	TRigger Board
TriDAS	Trigger and Data Acquisition System
TS	Track Segment
TSC	Trigger Sector Collector

TTC	Trigger Timing and Control
TTL	Transistor–Transistor Logic circuits operate with a 5-volt power supply
TTS	Trigger Throttle System
TWEEP	Topical Workshop on Electronics for Particle Physics
TX	Transmitter
UART	Universal Asynchronous Receiver-Transmitter
UDP	User Datagram Protocol (over Internet Protocol)
μGMT	micro Global Muon Trigger
μGT	micro Global Trigger
μROS	micro Read Out Server
USC55	Underground Services Cavern in building 55 at Point 5 (CMS)
μSD	micro Secure Digital card
μTCA	micro Telecommunications Computing Architecture
UXC55	Underground eXperimental Cavern in building 55 at Point 5 (CMS)
VCI	Vienna Conference on Instrumentation
VFE	Very Front-End
VHDCI	Very-High-Density Cable Interconnect
VHDL	VHSIC Hardware Description Language
VHSIC	Very-High Speed Integrated Circuit
VIO	Virtual Input / Output
VME	Versa Module Europa
VPT	Vacuum Photo Triodes
WLS	WaveLength Shifting
WS	Wedge Sorter
XML	eXtensible Markup Language
YB	iron Yoke in the Barrel
YE	iron Yoke Endcap disk

List of Figures

List of Tables

Part I

Εκτεταμένη σύνοψη

Περίληψη

Το σύστημα σκανδαλισμού του πειράματος "Συμπαγές Σωληνοειδές Μιονίων" (Compact Muon Solenoid, CMS) του Ευρωπαϊκού οργανισμού πυρηνικών ερευνών CERN (Conseil Européen pour la Recherche Nucléaire) αναβαθμίζεται συνεχώς έτσι ώστε να μπορεί να αντεπεξέλθει στην όλο και αυξανόμενη φωτεινότητα των αλληλεπιδράσεων αδρονίων. Η αναβάθμιση αυτή είναι προγραμματισμένο να γίνεται σε φάσεις, κατά τις οποίες το CMS διακόπτει την λειτουργία του. Οι φάσεις των αναβαθμίσεων του ηλεκτρονικού επιπέδου του συστήματος σκανδαλισμού (Level-1 Trigger, L1T) ξεκίνησαν το 2016 όπου και πραγματοποιήθηκε η πρώτη φάση αναβάθμισης. Το 2025 είναι προγραμματισμένο να συμβεί η δεύτερη φάση και στην συνέχεια ακολουθούν και άλλες φάσεις αναβαθμίσεων μετά το 2030.

Τμήμα του πρώτου επιπέδου σκανδαλισμού (δηλαδή αυτού που απαρτίζεται από ηλεκτρονικές μονάδες επεξεργασίας) της πρώτης φάσης της αναβάθμισης του πειράματος CMS περιγράφεται στην παρούσα Διδακτορική Διατριβή. Το κεντρικό ή βαρελοειδές σύστημα εύρεσης τροχιών μιονίων (Barrel Muon Track Finder, BMTF) αποτελεί το βασικό αντικείμενο που συνοψίζεται στις επόμενες ενότητες, οι οποίες συμπληρώνονται από την παρουσίαση εργασίας που αφορά και περισσότερα τμήματα του συστήματος σκανδαλισμού L1T. Έτσι εκτός από το BMTF παρουσιάζεται και εργασία που αφορά τρία συστήματα συλλογής και διανομής δεδομένων: TwinMux, Pre-Processing and Fan-out (CPPF) και AMC502. Καθώς επίσης και αξιολόγηση καλής λειτουργίας ηλεκτρονικών καρτών οι οποίες χρησιμοποιήθηκαν στο σύστημα ελέγχου και διανομής χρονισμού (Timing and Control Distribution System, TCDS).

Ο αλγόριθμος του BMTF αναπτύχθηκε με βάση αυτόν που λειτουργούσε έως το τέλος 2015 στο παλαιότερο σύστημα σκανδαλισμού το οποίο ονομάζεται Drift Tube Track Finder (DTTF). Στο νέο σύστημα, ο αλγόριθμος παρουσίασε ικανοποιητική απόδοση που επιβεβαιώθηκε μέσω συγκρίσεων που έγιναν με την απόδοση συστήματος απομίμησης του αλγόριθμου ανεπτυγμένου σε λογισμικό.

Κατά την διάρκεια της συναρμολόγησης του συστήματος στο πείραμα εγκαταστάθηκαν ηλεκτρονικές κάρτες, οπτικές ίνες αλλά και οπτικά μέσα, τμήμα των οποίων αντικαταστάθηκε λόγω μη ικανοποιητικής λειτουργίας τους. Κατά τις πρώτες δοκιμές το σύστημα παρουσίασε προβλήματα τα οποία λύθηκαν μέσα στα χρονικά περιθώρια που είχαν τεθεί και έτσι το BMTF τέθηκε σε πλήρη λειτουργία πριν το πείραμα CMS επαναλειτουργήσει για το 2016.

Εισαγωγή στην αναβάθμιση του συστήματος σκανδαλισμού των μιονίων

Το πείραμα "Συμπαγές Σωληνοειδές Μιονίων" ή Compact Muon Solenoid (CMS) είναι ένα από τα πειράματα που λαμβάνουν χώρα στο Ευρωπαϊκό Κέντρο Πυρηνικών ερευνών CERN) που βρίσκεται κοντά στη Γενεύη. Ο σκοπός του είναι η πειραματική μελέτη της Φυσικής Υψηλών Ενεργειών μέσω αλληλεπιδράσεων αδρονίων μετά από την επιτάχυνσή τους στο Μεγάλο Αδρονικό Επιταχυντή συγκρουομένων δεσμών (Large Hadron Collider, LHC).

Για κάθε αλληλεπίδραση οι ανιχνευτές του CMS παράγουν τεράστιο όγκο πληροφορίας μεγάλο μέρος της οποίας δεν είναι χρήσιμο στην ανάλυση των αποτελεσμάτων (π.χ. θόρυβος). Επιπλέον οι περισσότερες αλληλεπιδράσεις δεν προσφέρουν κάτι νέο ή κάτι χρήσιμο στην Φυσική και επομένως δεν είναι αναγκαίο να αποθηκευτούν για περαιτέρω ανάλυση.

Για τον λόγο αυτό έχει αναπτυχθεί ένα σύστημα επιλογής των χρήσιμων αλληλεπιδράσεων το οποίο καλείται σύστημα σκανδαλισμού (Trigger). Στο πείραμα CMS το σύστημα επιλογής υλοποιείται σε δύο επίπεδα.

Το πρώτο επίπεδο σκανδαλισμού (Level-1 Trigger, L1T) χρησιμοποιεί αποκλειστικά ηλεκτρονικές μονάδες επεξεργασίας, σχεδιασμένες ειδικά για το CMS. Το σύστημα L1T αποφασίζει μέσα σε 3.2 μs αν η πληροφορία που συλλέχθηκε από συγκρούσεις αδρονίων πρέπει να αποδοθεί στο δεύτερο επίπεδο σκανδαλισμού ή να απορριφθεί. Το L1T παρέχει κανάλια (κατηγορίες) σκανδαλισμού που αντιστοιχούν σε κατηγορίες σωματιδίων όπως πίδακες σωματιδίων αποτελούμενες από αδρόνια (jets), μεμονωμένα μιόνια (single muons), διπλά μιόνια (dimuons) και άλλα. Το σύστημα L1T λαμβάνει δεδομένα από τους ανιχνευτές με συχνότητα 40 MHz (δηλαδή την συχνότητα αλληλεπιδράσεων που παρέχει ο LHC) και αποδίδει τα αποτελέσματα στο δεύτερο επίπεδο σκανδαλισμού με συχνότητα 100 KHz.

Το δεύτερο επίπεδο σκανδαλισμού (High Level Trigger, HLT), μόλις λάβει από το L1T το σήμα σκανδαλισμού "Level-1 Accept" (L1A), διαβάζει και επεξεργάζεται την πληροφορία που προέρχεται απο το L1T στην συστοιχία υπολογιστών του (computer cluster). Το HLT επιλέγει τα γεγονότα που ικανοποιούν συγκεκριμένους κανόνες σκανδαλισμού οι οποίοι προκύπτουν ύστερα από αναλύσεις φυσικών ιδιοτήτων των τροχιών των σωματιδίων τα οποία προκύπτουν από τις αλληλεπιδράσεις. Από τις 40 x 10^6 αλληλεπιδράσεις το δευτερόλεπτο που αρχικά συμβαίνουν στο κέντρο του CMS ανά δευτερόλεπτο, το HLT επιλέγει τις 100 αλληλεπιδράσεις ανά δευτερόλεπτο τις περισσότερο ενδιαφέρουσες.

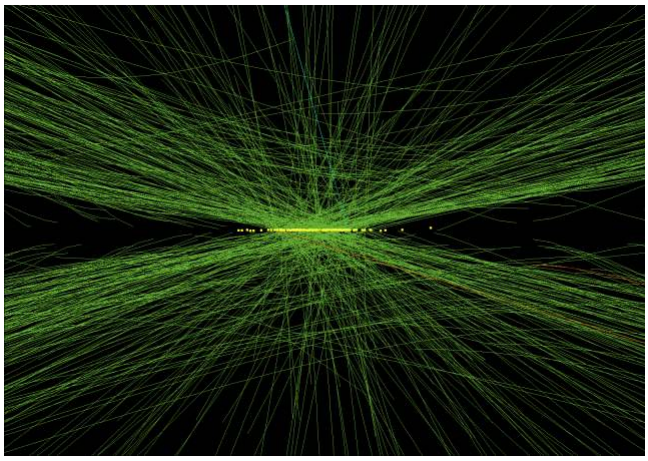
Το πρώτο επίπεδο σκανδαλισμού του CMS χωρίζεται σε ομάδες υποσυστημάτων σκανδαλισμού: τον σκανδαλισμό του καλοριμέτρου (calorimeter trigger) και τον σκανδαλισμό των μιονίων (muon trigger). Το δεύτερο απαρτίζεται χωρικά από ευρετές τροχιών μιονίων οι οποίοι λαμβάνουν δεδομένα τα όποια παράγονται στους τρεις τύπους ανιχνευτών μιονίων: θαλάμους ιονισμού με ηλεκτρόδια (άνοδο, κάθοδο), πλάκες υψηλής αντιστάσεως (Resistive Plate Chambers, RPC), ανιχνευτές θαλάμων ολίσθησης (Drift Tubes, DT) και τους ανιχνευτές θαλάμων καθοδικών λωρίδων (Cathode Strip Chamber, CSC).

Η ανάπτυξη του L1T του CMS ξεκίνησε το 2000 [1]. Είναι ικανό να λειτουργεί σε φωτεινότητα αλληλεπιδράσεων (luminosity: συντελεστής αναλογίας μεταξύ του ρυθμού των αλληλεπιδράσεων και του αντιστρόφου της ενεργούς διατομής, $\frac{dN}{dt}$=L/σ)

έως 10^{34} $cm^{-2}s^{-1}$. Το 2016 η luminosity αυξήθηκε στο 2 x 10^{34} $cm^{-2}s^{-1}$ και το 2025 μετά την δεύτερη φάση αναβάθμισης του επιταχυντή (Upgrade Phase II) θα φτάσει τα 7.5 x 10^{34} $cm^{-2}s^{-1}$. Η αύξηση της luminosity (εικόνα 1) αυξάνει τον ρυθμό των διαδοχικών συγκρούσεων που πραγματοποιούνται σχεδόν ταυτόχρονα (pile-up) όταν συναντώνται δύο αντίθετης κατεύθυνσης πακέτα πρωτονίων (colliding bunches). Το νέο περιβάλλον συγκρούσεων απαιτεί μεγαλύτερη αποδοτικότητα των ηλεκτρονικών μονάδων (efficiency), καλύτερη αξιοπιστία του υλικού και μείωση της συχνότητας σκανδαλισμού (trigger rate).

Όπως παρουσιάζεται στο τεχνικό δελτίο του αναβαθμισμένου συστήματος σκανδαλισμού (CMS Technical Design Report for the Level-1 Trigger Upgrade, CMS-TDR-12) η αποδοτικότητα είναι μεγαλύτερη και ο ρυθμός σκανδαλισμού μικρότερος όταν οι αλγόριθμοι χρησιμοποιούν πληροφορία από περισσότερους ανιχνευτές [2].

Πριν την αναβάθμιση του ηλεκτρονικού συστήματος σκανδαλισμού στην κεντρική περιοχή του CMS (κυλινδρικό κεντρικό τμήμα του CMS), οι αλγόριθμοι του συστήματος σκανδαλισμού των μιονίων χρησιμοποιούσαν δεδομένα μόνο από τους ανιχνευτές θαλάμων ολίσθησης (Drift Tubes, DT). Το 2016 το σύστημα L1T επανασχεδιάστηκε. Μέτα την αναβάθμιση αυτή το νέο σύστημα εύρεσης των μιονίων της κεντρικής περιοχής λαμβάνει πλέον δεδομένα και από το δεύτερο τύπο ανιχνευτών των μιονίων, τους θαλάμους ιονισμού με πλάκες υψηλής αντιστάσεως, Resistive Plate Chambers (RPC).



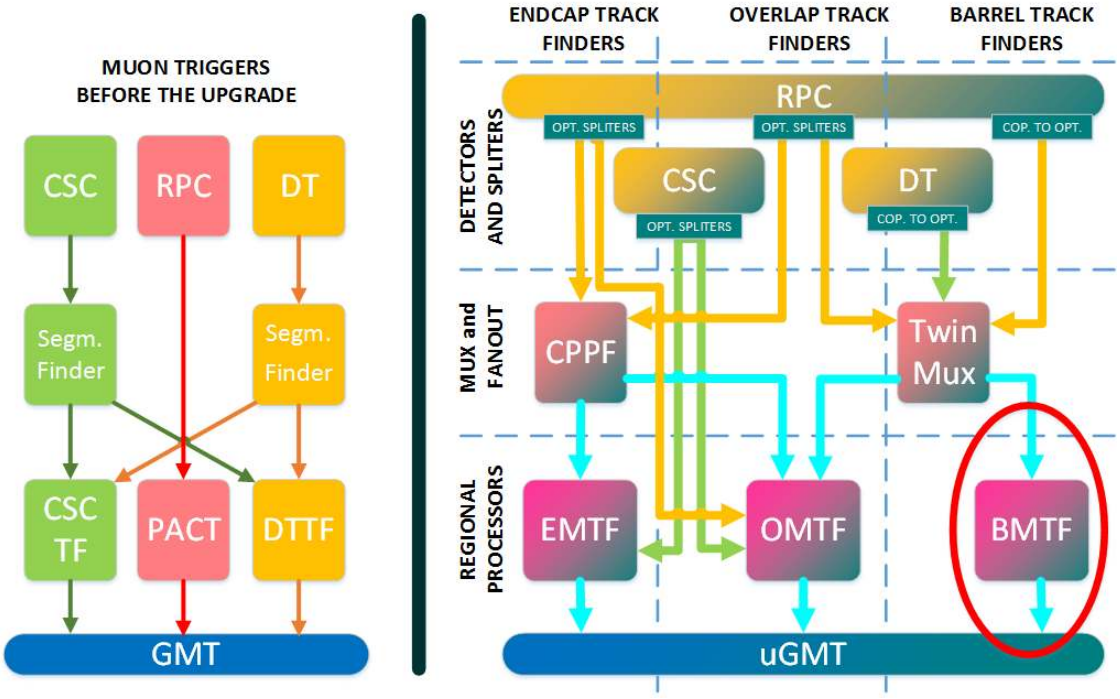
Εικόνα 1: Ανακατασκευή τροχιών φορτισμένων σωματιδίων σε αλληλεπίδραση p−p σε περιβάλλον υψηλού pile-up (υψηλή φωτεινότητα).

Στην εικόνα 2 φαίνεται η αλλαγή της αρχιτεκτονικής του ηλεκτρονικού συστήματος σκανδαλισμού των μιονίων από αρχιτεκτονική αλγόριθμου ανιχνευτών σε αρχιτεκτονική αλγόριθμου περιοχών.

Το σύστημα σκανδαλισμού των μιονίων περιλαμβάνει το σύστημα ανεύρεσης τροχιών στην κεντρική περιοχή ή περιοχή του κυλινδρικού κεντρικού τμήματος (Barrel Muon Track Finder, BMTF), το σύστημα ανεύρεσης τροχιών στην απομακρυσμένη περιοχή ή περιοχή καπακιών (Endcap Muon Track Finder, EMTF) και τέλος το σύστημα ανευρέσεως τροχιών στην κοινή περιοχή ή στην περιοχή επικαλύψεως (Overlap Muon Track Finder, OMTF).

Το BMTF λαμβάνει δεδομένα από το αναβαθμισμένο σύστημα συλλογής και

αρχικής επεξεργασίας δεδομένων TwinMux. Το EMTF λαμβάνει δεδομένα από το σύστημα συλλογής προ−επεξεργασίας και προώθησης δεδομένων, Concentration Pre-Processing and Fan-out (CPPF) και από τους ανιχνευτές θαλάμων καθοδικών λωρίδων, Cathode Strip Chamber (CSC). Το OMTF λαμβάνει δεδομένα από τα συστήματα CPPF και TwinMux καθώς επίσης και από τους ανιχνευτές CSC.



Εικόνα 2: Αριστερά παρουσιάζεται η αρχιτεκτονική του ηλεκτρονικού συστήματος σκανδαλισμού πριν από την αναβάθμισή του και δεξιά μετά από αυτήν.

Κεντρικό σύστημα σκανδαλισμού μιονίων

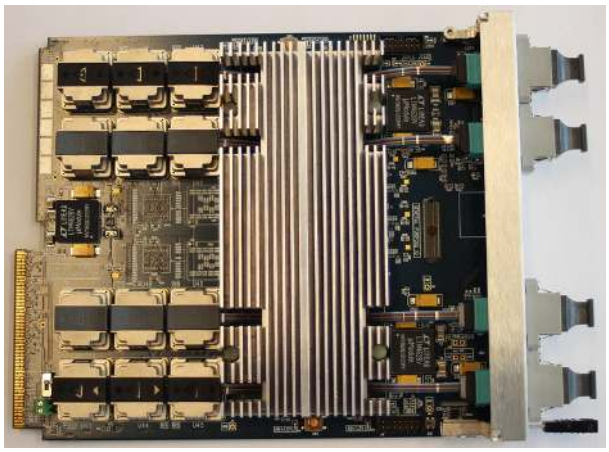
Όπως φαίνεται στο αριστερό μέρος της εικόνας 2, έως το 2015, το ηλεκτρονικό σύστημα, ανεύρεσης τροχιών των θαλάμων ολίσθησης σχεδιάστηκε ώστε να βρίσκει στην κεντρική περιοχή τροχιές μιονίων από δεδομένα των ανιχνευτών DT και στην περιοχή επικαλύψεως από τους ανιχνευτές CSC. Το σύστημα σκανδαλισμού προτύπων τροχιών μιονίων (PAttern Comparator Trigger, PACT) σχεδιάστηκε ώστε να βρίσκει τροχιές μιονίων στις ίδιες περιοχές. Στην συνέχεια, στο γενικό σύστημα σκανδαλισμού Global Muon Trigger (GMT) εφαρμοζόταν ένας αλγόριθμος επιλογής των καλύτερων μιονίων από τα δύο συστήματα.

Στο δεξιό μέρος της εικόνας 2 φαίνεται το αναβαθμισμένο σύστημα σκανδαλισμού των μιονίων και σε κύκλο το σύστημα BMTF που αντικατέστησε το DTTF και το PACT στην περιοχή του κυλινδρικού κεντρικού τμήματος του CMS. Το BMTF λαμβάνει δεδομένα από το σύστημα TwinMux. Το TwinMux συνδυάζει την πληροφορία της γωνίας και της θέσης των τροχιών των μιονίων από τους DTs και RPCs. Τα αποτελέσματα του συνδυασμού δίνουν στο BMTF παρόμοια αποδοτικότητα σε σύγκριση με το DTTF, χαμηλότερο ρυθμό σκανδαλισμού και μεγαλύτερη διακριτικότητα (granularity). Το BMTF στέλνει τα τρία καλύτερα μιόνια από κάθε επίμηκες σφηνοειδές τμήμα (wedge) του κυλινδρικού κεντρικού τμήματος του CMS, στο αναβαθμισμένο γενικό σύστημα σκανδαλισμού των μιονίων micro Glogal

Muon Trigger (μGMT). Το κάθε σφηνοειδές τμήμα εξυπηρετείται από μία κάρτα MP7. Ο μέγιστος αριθμός των μιονίων από τις συνολικά δώδεκα κάρτες BMTF που προωθούνται για περαιτέρω ανάλυση είναι 36. Τελικά από τα αυτά τα μιόνια η επόμενη μονάδα σκανδαλισμού μGMT, επιλέγει τα τέσσερα καλύτερα.

Το ηλεκτρονικό υλικό του συστήματος σκανδαλισμού της κεντρικής περιοχής

Το σύστημα BMTF χρησιμοποιεί μοντέρνα τεχνολογία που ήδη χρησιμοποιείται σε τηλεπικοινωνιακά συστήματα και παρέχει αξιοπιστία και υψηλή ισχύ επεξεργασίας. Το σύστημα σκανδαλισμού BMTF υλοποιήθηκε στο τηλεπικοινωνιακό πρότυπο micro Telecommunications Computing Architecture (μTCA) αντικαθιστώντας έτσι το απαρχαιωμένο πρότυπο Versa Module Europa (VME), που χρησιμοποιήθηκε στο DTTF πριν από την αναβάθμιση. Η λογική που χρησιμοποιείται στο BMTF σχεδιάστηκε και υλοποιήθηκε σε προγραμματιζόμενο ολοκληρωμένο κύκλωμα τύπου Field-Programmable Gate Array (FPGA) της σειράς Virtex7 της εταιρίας Xilinx. Το FPGA αυτό υπερκαλύπτει τις απαιτήσεις του αναβαθμισμένου DTTF τόσο στην ταχύτητα όσο και στους απαιτούμενους πόρους (logic slices, block memories, DSPs, MMCMs, Look Up Tables κ.α.). Το BMTF χρησιμοποιεί 12 κάρτες Master Proccesor Virtex-7 (MP7). Η MP7 είναι μία κάρτα τύπου Advanced Mezzanie Card (AMC) και φαίνεται στην εικόνα 3. Έχει σχεδιαστεί στο Imperial College και χρησιμοποιείται ευρέως στο πείραμα CMS [3]. Στο σύστημα BMTF κάθε κάρτα MP7 καλύπτει το 1/12 της κεντρικής περιοχής του κυλινδρικού κεντρικού τμήματος του CMS ή ενός σφηνοειδούς τμήματος (wedge) και αποτελείται από πέντε τομείς (Sectors) ανιχνευτών DT και RPC κατά μήκος της διεύθυνσης της δέσμης πρωτονίων. Το υλικό της MP7 περιέχει μεταξύ άλλων: κυκλώματα χρονισμού χωρίς θόρυβο (Phase Locked Loop, PLL) που παρέχουν στο FPGA ρολόι χαμηλής διακύμανσης στο χρόνο ανόδου και καθόδου (low jitter), μικροελεγκτή (MMC) της εταιρίας Atmel ο οποίος ελέγχει την ομαλή τροφοδοσία της κάρτας, μέσον αποθήκευσης και φόρτωσης λογικής τύπου micro Secure Digital (μSD) και 12 οπτικά συστήματα minipods τα οποία μετατρέπουν το ηλεκτρικό σήμα σε οπτικό και συνολικά παρέχουν ταχύτητα 72 x 10 Gb/s οπτικών καναλιών.



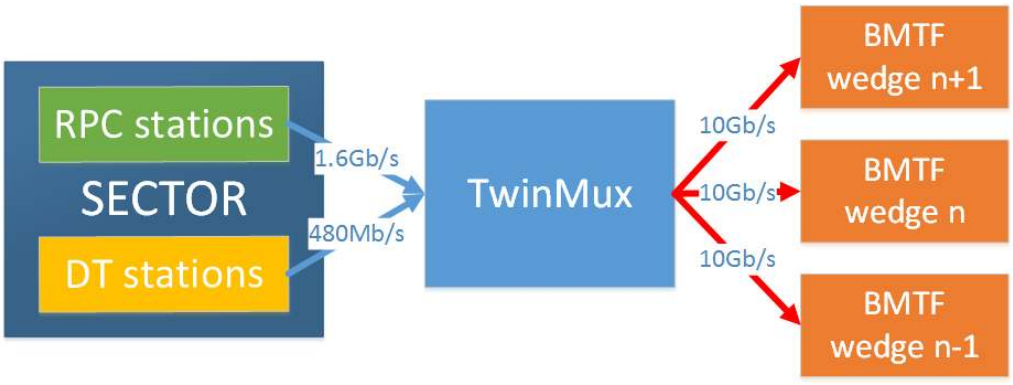
Εικόνα 3: Master Processor - Virtex-7 (MP7)

Στην εικόνα 4 παρουσιάζεται το ηλεκτρονικό πλαίσιο (μTCA crate) του συστήματος BMTF το οποίο μέσω των 6 MP7s χρησιμοποιείται στον σκανδαλισμό μιονίων των άνω 6 σφηνοειδών τμημάτων. Στα αριστερά βρίσκεται η κάρτα ελέγχου και εξυπηρέτησης του συστήματος η οποία καλείται μεταγωγέας και διαχειριστής δεδομένων του πλαισίου (MicroTCA Carrier Hub, MCH). Στα δεξιά υπάρχει η κάρτα AMC13, η οποία από την μία διανέμει τον χρονισμό του LHC και βασικές εντολές όπως: "λειτούργησε", "σταμάτησε την λειτουργία" στις MP7s και από την άλλη συλλέγει δεδομένα από τις MP7s, τα πακετάρει και τα στέλνει στο σύστημα συλλογής δεδομένων, Data AcQuisition (DAQ).

Εικόνα 4: Το σύστημα BMTF των Wedges 1,2,3,4,5,6

Ο αλγόριθμος του BMTF

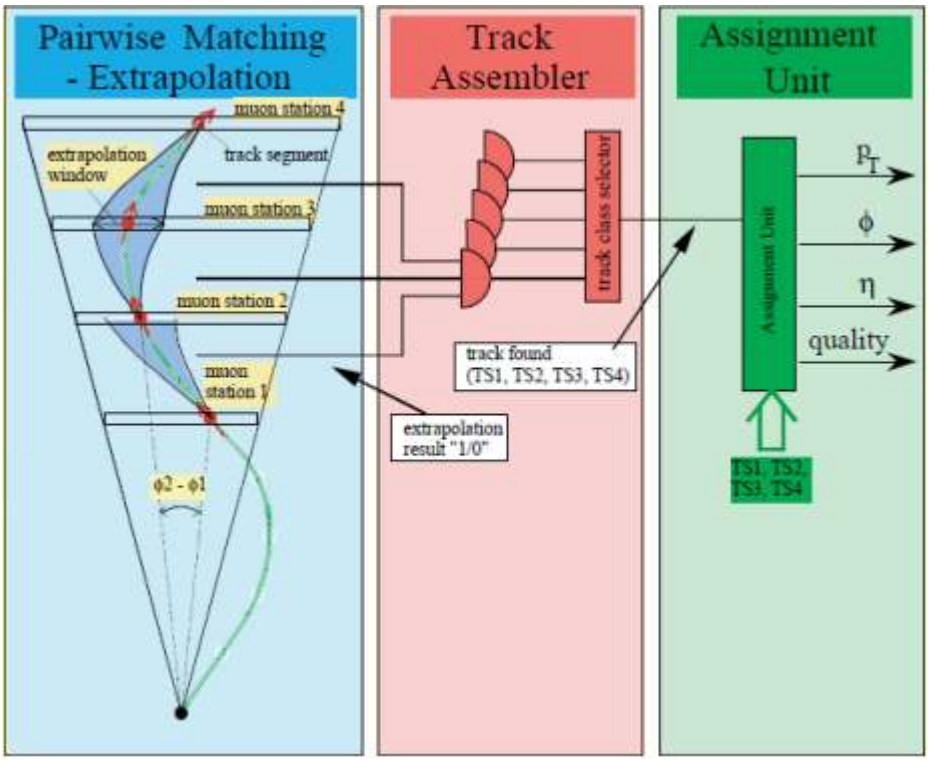
Το σύστημα σκανδαλισμού των μιονίων της κεντρικής περιοχής του CMS ομαδοποιεί τους ανιχνευτές σε 12 σφηνοειδή τμήματα. Το κάθ' ένα από αυτά αποτελείται από 5 τομείς (sectors) και κάθε sector αποτελείται από ανιχνευτές που καλούνται σταθμοί μιονίων (muon stations) και αποτελούνται από 4 DTs και 3 RPCs. Οι ηλεκτρονικές μονάδες που βρίσκονται ενσωματωμένες στο πίσω μέρος των ανιχνευτών αυτών, μέσα σε ηλεκτρονικό σασί (minicrate), μετατρέπουν τα αναλογικά σήματα των αντίστοιχων DTs και των RPCs σε ψηφιακή πληροφορία η οποία αποκαλείται trigger primitives. Τα δεδομένα αυτά φτάνουν στις κάρτες πολυπλεξίας και διανομής TwimMux [4].



Εικόνα 5: TwinMux - Κάρτα συλλογής και διανομής δεδομένων ενός sector

Στις κάρτες TwinMux εφαρμόζεται ένας αλγόριθμος εμπλουτισμού της πληροφορίας που συμπληρώνει τα primitives των DTs με δεδομένα από τα 3 RPCs του ίδιου τομέα (sector), όταν τα ενεργά DTs είναι λιγότερα από 4. Τα δεδομένα που προκύπτουν από τον αλγόριθμο εμπλουτισμού του συστήματος TwinMux καλούνται superprimitives. Όπως φαίνεται και στην εικόνα 5, η κάθε κάρτα TwinMux εξυπηρετεί έναν τομέα (sector) ανιχνευτών και στέλνει τα ίδια δεδομένα σε τρεις κάρτες BMTF (fan-out). Το fan-out γίνεται με τέτοιο τρόπο, ώστε ο αλγόριθμος του συστήματος BMTF να βρίσκει τροχιές μιονίων τα οποία διέρχονται από γειτονικά sectors.

Το σύστημα BMTF χρησιμοποιεί τα δεδομένα από τους ανιχνευτές της κεντρικής περιοχής με ψευδοωκύτητα $|\eta| < 0.85$. Η θέση που βρέθηκε το μιόνιο, η γωνία ϕ, η διεύθυνση η που είχε, καθώς και η ακρίβεια των μετρήσεων συνθέτουν την τελική πληροφορία (αριστερό τμήμα της εικόνας 6). Η ακρίβεια των μετρήσεων εκφράζεται με τα (δυαδικά) ψηφία ποιότητας (quality bits). Ο αλγόριθμος του συστήματος BMTF χρησιμοποιεί την πληροφορία της εισόδου για να ανακατασκευάσει τις τροχιές των μιονίων και να αποκλείσει αυτές που δεν ικανοποιούν τις συνθήκες που προσδιορίσθηκαν με προσομοίωση (μεσαίο τμήμα της εικόνας 6). Από τις τροχιές που προκύπτουν το σύστημα BMTF υπολογίζει τις φυσικές παραμέτρους των υποψήφιων μιονίων (δεξιό τμήμα της εικόνας 6). Από την καμπύλωση της τροχιάς υπολογίζεται η εγκάρσια ορμή και από τα σημεία που περνάει το μιόνιο προσδιορίζεται η αρχική διεύθυνσή του. Τέλος από το πλήθος και την ταυτότητα των ανιχνευτών που κατέγραψαν την τροχιά υπολογίζεται η ποιότητα της τροχιάς (quality bits και track address). Ο αλγόριθμος χωρίζεται σε τρεις ηλεκτρονικές μονάδες [5]:



Εικόνα 6: Ο αλγόριθμος σκανδαλισμού των μιονίων της περιοχής $|\eta|$ <0.85 - BMTF

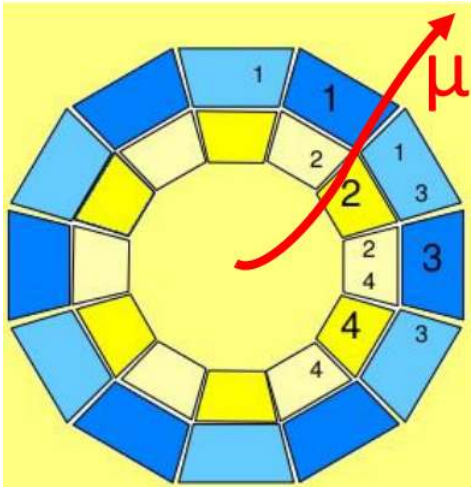
1. Η πρώτη ηλεκτρονική μονάδα καλείται μονάδα προέκτασης με βάση τα υπάρχοντα στοιχεία προβολής (Extrapolator unit). Σε αυτήν χρησιμοποιούνται, η θέση, η διεύθυνση και η ακρίβεια, που βρέθηκαν σε διαφορετικούς θαλάμους DT του

κεντρικού τομέα (own sector). Με τη χρήση πινάκων αντιστοίχισης, Look Up Tables (LUTs) το υποψήφιο μιόνιο προβάλλεται στον επόμενο θάλαμο δηλαδή ελέγχεται αν υπάρχει σήμα αντίστοιχο του μιονίου στον επόμενο θάλαμο. Ο αλγόριθμος ελέγχει αν η προέκταση αυτή είναι εντός ενός αποδεκτού παραθύρου, αν όχι αυτό το τμήμα της τροχιάς απορρίπτεται. Ο ίδιος αλγόριθμος λειτουργεί παράλληλα στους γειτονικούς τομείς.

2. Η δεύτερη ηλεκτρονική μονάδα καλείται μονάδα συναρμολόγησης της τροχιάς (Track Assembler Unit). Σε αυτήν, τα αποδεκτά επιμέρους τμήματα των τροχιών της προηγούμενης μονάδας συνθέτουν μία πλήρη τροχιά με την αντίστοιχη ποιότητα (track address).

3. Η τρίτη ηλεκτρονική μονάδα καλείται μονάδα αντιστοίχισης (Assignment Unit). Ομοίως με την πρώτη μονάδα και σε αυτήν χρησιμοποιούνται πίνακες αντιστοίχισης (LUTs), οι οποίοι παίρνουν τη διεύθυνσή τους από την έξοδο της προηγούμενης μονάδας και παρέχουν τις αντίστοιχες φυσικές παραμέτρους. Κατ' αυτόν τον τρόπο, μέσω αυτής της μονάδας, ο αλγόριθμος εξάγει την εγκάρσια ορμή (p_T), την διεύθυνση (ϕ) και την τιμή της ψευδοωκύτητας (η) της τροχιάς.

Κάθε κάρτα MP7 βρίσκει τροχιές μιονίων που περνούν από τουλάχιστον δύο θαλάμους ολίσθησης των μιονίων (DT). Οι τροχιές αυτές μπορεί να προέρχονται τόσο από γειτονικούς στο ϕ θαλάμους (γειτονικές σφήνες) όσο και από γειτονικούς στο η θαλάμους. Στην εικόνα 7 φαίνεται το παράδειγμα μιας τροχιάς που περνάει από γειτονικές σφήνες. Στο συγκεκριμένο παράδειγμα ο επεξεργαστής της σφήνας 2 αναζητά τροχιές μιονίων. Για να ανακατασκευάσει την τροχιά λαμβάνει δεδομένα και από τις σφήνες 1 και 3. Ο αλγόριθμος λειτουργεί παράλληλα για όλες τις σφήνες. Κάθε μία από τις δώδεκα κάρτες στέλνει τα τρία καλύτερα υποψήφια μιόνια στο αναβαθμισμένο σύστημα γενικού σκανδαλισμού των μιονίων μGMT. Το τελευταίο κάνει την γενική ταξινόμηση των υποψήφιων μιονίων που προέρχονται από όλες τις περιοχές ανιχνευτών του CMS, δηλαδή από τα συστήματα του BMTF, του OMTF και του EMTF. Το μGMT ακυρώνει κάθε φορά ένα εκ των δυο ίδιων μιονίων που προκύπτουν από δυο διαφορετικά συστήματα (π.χ. BMTF και OMTF), λόγω αλληλοκάλυψης της περιοχής και κρατάει έως 4 μιόνια από την περιοχή του βαρελιού.

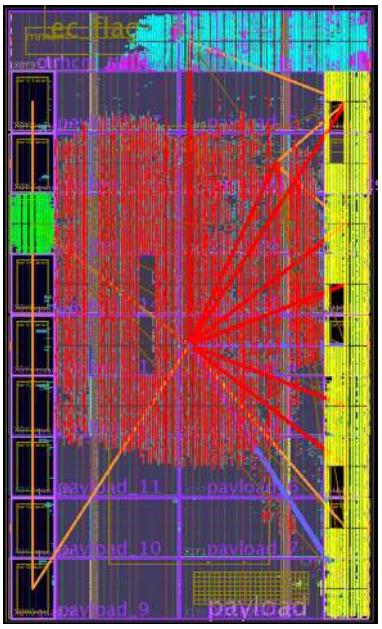


Εικόνα 7: Τροχιά μιονίου εισερχόμενη σε γειτονικούς θαλάμους.

Εφαρμογή της λογικής του συστήματος σκανδαλισμού του κυλινδρικού κεντρικού τμήματος του CMS στο ολοκληρωμένο κύκλωμα virtex-7 της κάρτας MP7

Ο αλγόριθμος του συστήματος καθώς και η λογική του γενικού ελέγχου της κάρτας, του κυκλώματος χρονισμού, των διεπαφών (I^2C, SPI, IPbus), του ασύγχρονου πρωτόκολλου επικοινωνίας ταχύτητας 10 Gb/s, της λογικής μορφοποίησης δεδομένων και της αποστολής στο σύστημα δειγματοληψίας, συνθέτουν το σύνολο των διασυνδέσεων (netlist) ηλεκτρονικών λογικών πυλών, πινάκων αντιστοίχισης (Look-Up Tables), μνημών, κυκλωμάτων χρονισμού (PLLs), σειριακών πομποδεκτών (transceivers) και ενισχυτών. Το netlist που προέκυψε από την λογική που χρησιμοποιείται στο προγραμματιζόμενο ολοκληρωμένο κύκλωμα virtex-7 του BMTF, τροποποιήθηκε έτσι ώστε να ικανοποιεί τους χωρικούς και χρονικούς περιορισμούς που τίθενται από την αρχιτεκτονική της σειράς 7 ολοκληρωμένων κυκλωμάτων της εταιρίας Xilinx, από τους πόρους που διαθέτει το συγκεκριμένο FPGA αλλά και από την απαίτηση που τέθηκε για μικρότερο χρόνο επεξεργασίας των δεδομένων και του ελάχιστου δυνατού χρόνου απόκρισης του συστήματος BMTF.

Αρχικά ο χρόνος επεξεργασίας των δεδομένων του συστήματος BMTF ήταν ίσος με χρόνο 20 αλληλεπιδράσεων (bunch Crossings, BXs) πρωτονίων στο CMS ο οποίος είναι μεγαλύτερος από αυτόν που ορίστηκε για το σύστημα και έτσι δεν ήταν δυνατή η χρήση του. Μετά από τροποποιήσεις που έγιναν στην λογική και στο σύνολο των διασυνδέσεων που προέκυψε, ο χρόνος επεξεργασίας του αλγόριθμου μειώθηκε στα 6 BXs. Η μείωση αυτή βασίστηκε στην αντικατάσταση του ρολογιού του αλγόριθμου (40MHz), με ρολόι (160MHz) και στον επανασχεδιασμό του netlist. Επίσης τμήματα του αλγόριθμου όπως αυτό της κατάταξης των μιονίων σε σειρά προτεραιότητας σχεδιάστηκαν από την αρχή έτσι ώστε να παράγεται το ίδιο αποτέλεσμα αλλά και συγχρόνως να αφαιρεθούν τμήματα που δημιουργούσαν καθυστέρηση σε σήματα απόκρισης.



Εικόνα 8: Εφαρμογή της λογικής στο FPGA.

Το netlist του BMTF οργανώθηκε σε τμήματα και αυτά οριοθετήθηκαν σε περιοχές του FPGA οι οποίες φαίνονται στην εικόνα 8. Στο κίτρινο τμήμα περιορίστηκε η λογική που περιέχει τους σειριακούς δέκτες με το ασύγχρονο πρωτόκολλο επικοινωνίας και μνήμες εισόδου. Στο πράσινο τμήμα περιορίστηκε η λογική που περιέχει τους σειριακούς πομπούς και αντίστοιχα το ασύγχρονο πρωτόκολλο επικοινωνίας και μνήμες εξόδου. Στο κεντρικό ή κόκκινο τμήμα βρίσκεται εφαρμοσμένη η λογική του BMTF. Στο μπλε τμήμα εφαρμόζεται η λογική συλλογής δεδομένων (DAQ) και στο μοβ η βασική λογική ελέγχου της κάρτας.

Η τελική εκδοχή της εφαρμογής της λογικής του BMTF δεσμεύει το ένα τρίτο των διαθέσιμων ηλεκτρονικών πόρων γεγονός που επιτρέπει την περαιτέρω αναβάθμισή του.

Προσαρμογή της λογικής που αναπτύχθηκε για την ηλεκτρονική κάρτα MP7 σε κάρτες του CMS L1T έκτός του BMTF

Η λογική που υλοποιήθηκε στο σύστημα BMTF βασίστηκε στο υλικολογισμικό (firmware) της MP7 κάρτας, η οποία υλοποιήθηκε στο FPGA xc7vx690tffg1927-2 της σειράς virtex-7. Στην λογική της MP7 προσαρμόστηκε ο αλγόριθμος του συστήματος έτσι ώστε να συνεργάζεται με αυτήν. Το firmware της MP7 περιέχει την βασική λογική η οποία απαρτίζεται από τα παρακάτω τμήματα (blocks):

1. Βασική λογική (Infrastructure block). Παρέχει την διεπαφή IPbus και την αντίστοιχη λογική, με την οποία ελέγχεται η κάρτα και ο αλγόριθμός που εφαρμόζει. Επίσης περιέχει μοντέρνο κύκλωμα χρονισμού PLLs που στην οικογένεια ολοκληρωμένων Virtex7 καλούνται MMCM (Mixed-Mode Clock Manager).

2. Τμήμα χρονισμού (Timing Trigger Control, TTC). Έλεγχος του συστήματος σκανδαλισμού από το σύστημα σκανδαλισμού, ελέγχου και διανομής του χρονισμού (Trigger, Control and Distribution System, TCDS) μέσω βασικών εντολών "ξεκίνα", "σταμάτα" και "συγχρόνισε την λειτουργία" (BGo commands) και ανάκτηση του χρονισμού LHC στο τοπικό σύστημα (TwinMux, CPPF, AMC502) μέσω του TCDS.

3. Τμήμα μορφοποίησης δεδομένων (Formatters block). Περιλαμβάνει μορφοποίηση και πακετάρισμα των δεδομένων για την αποστολή τους μέσω οπτικών ινών στο επόμενο σύστημα σκανδαλισμού.

4. Τμήμα λήψης και αποστολής δεδομένων (Datapath block). Περιλαμβάνει ασύγχρονη διεπαφή σειριακών ζεύξεων ταχύτητας 10 Gb/s για αποστολή δεδομένων σε οπτικές ίνες και μνήμες πολλαπλής χρήσης που χρησιμοποιούνται για λήψη και αποστολή δεδομένων.

5. Τμήμα αποστολής στο σύστημα δειγματοληψίας DAQ. (Readout block). Περιλαμβάνει διεπαφή του συστήματος με το σύστημα συλλογής δεδομένων (DAQ). Μόλις το σύστημα BMTF λάβει το σήμα L1A, η λογική συλλέγει τα δεδομένα εισόδου και εξόδου του συστήματος, τα πακετάρει προσθέτοντας επικεφαλίδα (header) και ακολουθία δεδομένων (trailer) και τα αποστέλλει στον DAQ.

Η λογική που σχεδιάστηκε για την κάρτα MP7 επανασχεδιάστηκε και προσαρμόστηκε σε τρία ακόμα υποσυστήματα του συστήματος σκανδαλισμού L1T του CMS, τα οποία χρησιμοποιούν διαφορετικό υλικό (hardware). Στην εικόνα 9 παρουσιάζεται το hardware των συστημάτων αυτών. Στα αριστερά φαίνεται η κάρτα του συστήματος TwinMux που βασίζεται στο FPGA xc7vx330tffg1761-3 της σειράς virtex-7 της Xilinx. Στην μέση απεικονίζεται η κάρτα του συστήματος CPPF που βασίζεται σε δύο FPGAs. Το ένα είναι το xc7vx415tffg1158-2 της σειράς virtex-7 και το άλλο είναι το xc7k70tfbg484-2 της σειράς kintex-7 της Xilinx. Στα δεξιά φαίνεται το hardware του συστήματος AMC502 που βασίζεται στο FPGA xc7k420tffg1156-2 της σειράς kintex-7. Ξεκινώντας από την λογική που αναπτύχθηκε για το FPGAs της MP7

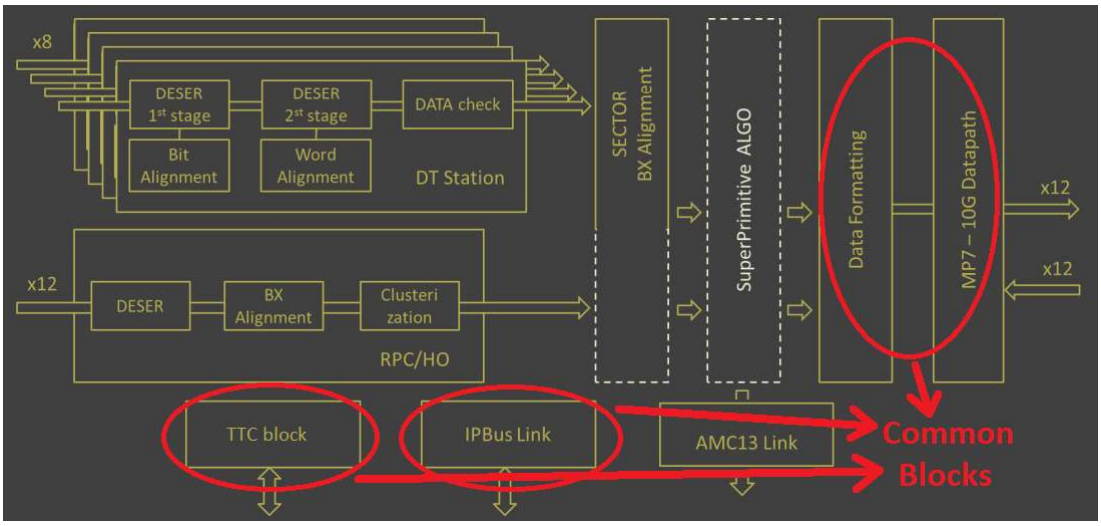
και αφαιρώντας τα τμήματα του κώδικα VHDL που χρησιμοποιούνται στην επικοινωνία του FPGA με το υλικό της κάρτας MP7, δημιουργήθηκε ένα βασικό ηλεκτρονικό σχέδιο, το οποίο χρησιμοποιήθηκε στην ανάπτυξη λογικής και για τις κάρτες των συστημάτων TwinMux, CPPF και AMC502.

(a) TwinMux (b) CPPF (c) AMC502

Εικόνα 9: Ηλεκτρονικές κάρτες, στις οποίες εφαρμόστηκε λογική η οποία αναπτύχθηκε με βάση αυτήν που σχεδιάστηκε στην κάρτα MP7

Ανάπτυξη κώδικα VHDL για την κάρτα TwinMux

Στην εικόνα 10 φαίνεται η λογική που χρησιμοποιεί η κάρτα TwinMux και σε κόκκινο κύκλο τα τμήματα που αντιγράφηκαν και ενσωματώθηκαν από την MP7.



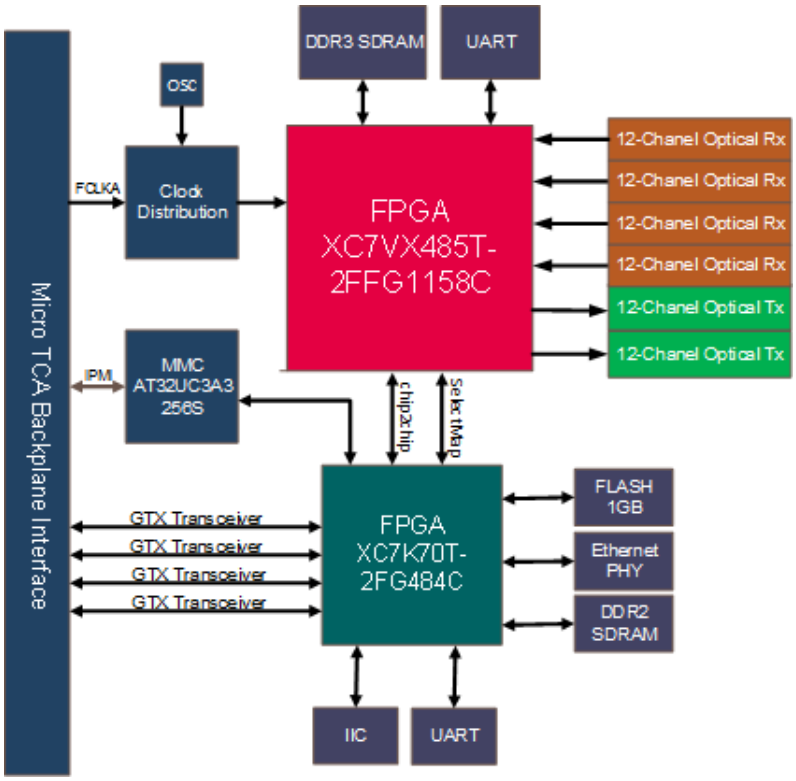
Εικόνα 10: Τα TwinMux και τα κοινά με την MP7 blocks

Η κάρτα TwinMux χρησιμοποιεί FPGA ίδιας αρχιτεκτονικής με αυτήν της κάρτας MP7 αλλά διαθέτει περίπου τους μισούς πόρους. Επίσης το FPGA της TwinMux είναι ταχύτερο (speed grade 3), γεγονός που του επιτρέπει να χρησιμοποιεί πολλαπλάσια ταχύτητα λήψης δεδομένων (oversampling). Η TwinMux χρησιμοποιεί τα ακόλουθα τμήματα σχεδιασμένα αρχικά για την κάρτα MP7. Περιέχεται το τμήμα λογικής

χρονισμού (TTC) έτσι ώστε το σύστημα να ελέγχεται από το TCDS και να λαμβάνει το ρολόι του LHC. Επίσης χρησιμοποιεί την βασική λογική (infrastructure), όπου μέσω της διεπαφής IPbus χρησιμοποιεί διεύθυνση IP-UDP, η οποία ελέγχεται από τον χρήστη. Τέλος χρησιμοποιεί τα τμήματα μορφοποίησης, ανάκτησης και αποστολής δεδομένων (formatters και datapath), με τα οποία εφαρμόζει ασύγχρονο πρωτόκολλο επικοινωνίας ταχύτητας 10 Gb/s και μέσω 12 οπτικών καναλιών τα δεδομένα αποστέλλονται στα συστήματα BMTF και OMTF.

Ανάπτυξη κώδικα VHDL για την κάρτα CPPF

Στην εικόνα 11 φαίνεται το διάγραμμα του υλικού της κάρτας CPPF και των διασυνδέσεών της. Η κάρτα χρησιμοποιεί δύο FPGAs. Το μικρότερο είναι Kintex-7 της Xilinx και ελέγχει την κάρτα χρησιμοποιώντας διεπαφές IPbus, I^2C, UART, Ethernet, DDR3 και SPI. Το σύστημα διαβάζει αισθητήρες θερμοκρασίας και στέλνει τις τιμές στον μικροελεγκτή (MMC) της κάρτας. Ο MMC επικοινωνεί με το backplane του μTCA χρησιμοποιώντας το πρωτόκολλο IPMI και κάνει την διαχείριση της παρεχόμενης ισχύος. Το μεγαλύτερο FPGA τύπου Virtex-7, περιέχει διεπαφές DDR3, UART. Χρησιμοποιούνται 16 κανάλια εισόδων, ταχύτητας 1.6 Gb/s στα οποία παρέχονται δεδομένα από τους ανιχνευτές RPC, καθώς επίσης και 8 κανάλια εξόδου όπου χρησιμοποιείται ασύγχρονο πρωτόκολλο επικοινωνίας ταχύτητας 10 Gb/s μέσω του οποίου στέλνονται τα δεδομένα στο σύστημα OMTF.



Εικόνα 11: Λογικό διάγραμμα και διασυνδέσεις του υλικού της κάρτας CPPF.

Το firmware που αναπτύχθηκε για την κάρτα CPPF διαμορφώθηκε σε δύο FPGA. Η βασική λογική (infrastructure) ενσωματώθηκε στο FPGA kintex-7 και όλα τα υπόλοιπα στο Virtex-7. Μεταξύ των δύο αναπτύχθηκε παράλληλο πρωτόκολλο 8 bit με το οποίο το IPbus αποκτά πρόσβαση στα τμήματα της λογικής του Virtex-7. Το FPGA

Virtex-7 περιέχει το τμήμα λογικής χρονισμού (TTC), τα τμήματα μορφοποίησης, ανάκτησης και αποστολής δεδομένων (formatters και datapath) έτσι ώστε το σύστημα να ελέγχεται από το TCDS και να στέλνει τα δεδομένα από τα κανάλια εξόδου στο σύστημα OMTF. Τέλος, σε αντίθεση με τη κάρτα TwinMux, η CPPF χρησιμοποιεί το τμήμα ανάγνωσης δεδομένων (readout) της MP7, έτσι ώστε να στέλνει δεδομένα στο σύστημα DAQ.

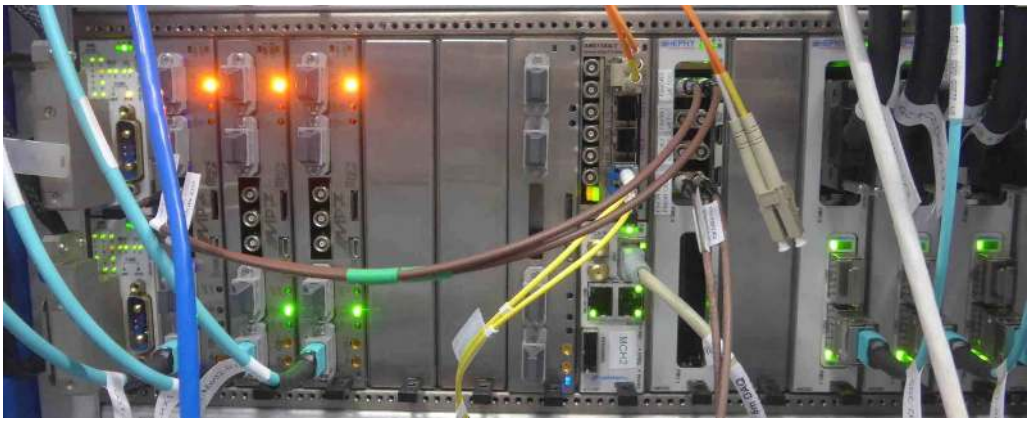
Ανάπτυξη κώδικα VHDL για την κάρτα AMC502

Η κάρτα AMC502 προοριζόταν για δύο χρήσεις. Η πρώτη ήταν η χρήση της ως εφεδρικό σύστημα στην περίπτωση που κατά την αναβάθμιση οι αλγόριθμοι μιονίων αποτύγχαναν να χρησιμοποιήσουν τα δεδομένα από τους ανιχνευτές RPC. Σε εκείνη την περίπτωση το σύστημα σκανδαλισμού PAttern Comparator Trigger (PACT), που χρησιμοποιούνταν πριν την αναβάθμιση και έβρισκε τροχιές μιονίων μέσω των ανιχνευτών RPC, θα παρέμενε σε λειτουργία. Τότε η κάρτα αυτή θα προωθούσε τα αποτελέσματα του PACT στο γενικό σύστημα σκανδαλισμού των μιονίων μGMT. Η δεύτερη χρήση της κάρτας AMC502, η οποία και τελικά υιοθετήθηκε, ήταν η αναμετάδοση δεδομένων σκανδαλισμού (technical bits) από το σύστημα γενικού σκανδαλισμού πριν την αναβάθμιση GT στο αναβαθμισμένο σύστημα μGT. Η κάρτα AMC502 αντί για μικροελεκτή περιέχει τον επεξεργαστή iMX6 Quad CPU της Freescale Semiconductor Inc, ο οποίος υποστηρίζει λειτουργικό σύστημα Fedora και χρησιμοποιείται στην διαχείριση των κυκλωμάτων ισχύος της κάρτας και στον προγραμματισμό του FPGA.

Εικόνα 12: Η κάρτα AMC502 με τις δύο κάρτες FMC.

Όπως φαίνεται στην εικόνα 12, η κάρτα AMC502 είναι τύπου μητρικής κάρτας (carrier) και έχει δύο υποδοχές για δύο θυγατρικές κάρτες τύπου FPGA Mezzanine Card (FMC). Η δεξιά FMC που σχεδιάστηκε από το ινστιτούτο της Βιέννης (Institute of High Energy Physics, HEPHY) λαμβάνει δεδομένα χρησιμοποιώντας παράλληλο πρωτόκολλο ταχύτητας 480 Mb/s. Στα αριστερά φαίνεται η κάρτα F14 η οποία σχεδιάστηκε από την εταιρία Faster Technoogy και στέλνει δεδομένα με οπτικά μέσα (SFPs) με ταχύτητα 10 Gb/s. Το FPGA Kintex-7 της κάρτας AMC502

είναι διαφορετικής αρχιτεκτονικής από αυτήν της κάρτας MP7 (Virtex-7). Έτσι τα τμήματα που αναπτύχθηκαν αρχικά για την MP7 χρειάστηκαν αρκετές τροποποιήσεις για να προσαρμοστούν στην νέα αρχιτεκτονική. Ειδικότερα η λογική που ελέγχει τα ηλεκτρονικά στοιχεία tranceivers αντικαταστάθηκε και αναπτύχθηκε εξ αρχής. Στην AMC502 προσαρμόστηκαν τα τμήματα βασικής λογικής (infrastructure), το τμήμα λογικής χρονισμού (TTC), τα τμήματα μορφοποίησης, ανάκτησης και αποστολής δεδομένων (formatters και datapath) και το τμήμα ανάγνωσης δεδομένων (readout). Στην εικόνα 13 φαίνεται το πλαίσιο του συστήματος μGT και δεξιά οι τρεις AMC502 που χρησιμοποιήθηκαν σε αυτό.



Εικόνα 13: Το πλαίσιο του συστήματος micro Global Trigger, μGT.

Στην εικόνα 14 παρουσιάζονται οι ηλεκτρονικές κάρτες και το πλαίσιο στο CERN όπου αναπτύχθηκε λογική για τα συστήματα, BMTF, Twinmux, CPPF και AMC502.

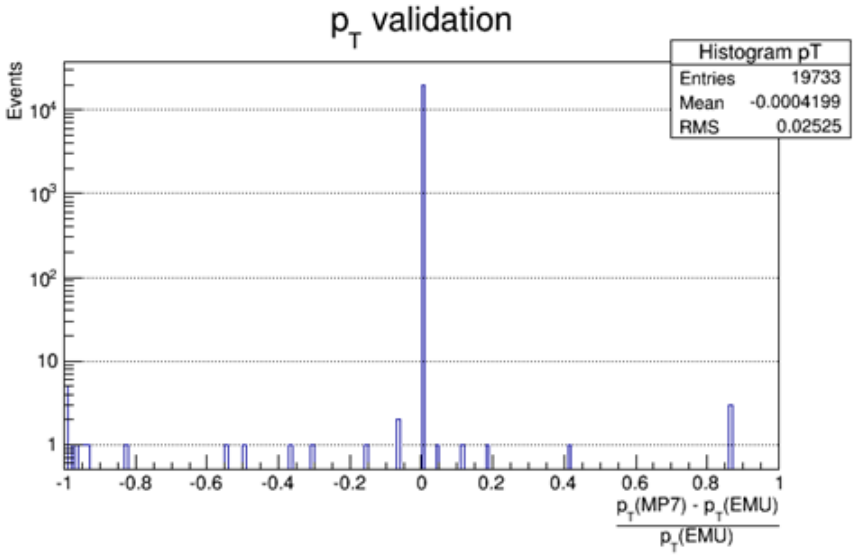
Εικόνα 14: Πειραματικό ηλεκτρονικό πλαίσιο. Από αριστερά προς τα δεξιά περιέχει τις κάρτες: Δύο MP7, μία AMC502, δύο MP7, μία TwinMux, μία AMC13 και μία MCH, μία MP7 και δύο CPPF.

Έλεγχος σωστής λειτουργίας αλγόριθμου σκανδαλισμού μιονίων BMTF

Για την αξιολόγηση της σωστής λειτουργίας του BMTF χρησιμοποιήθηκαν δεδομένα από πρότυπο προσομοίωσης Monte Carlo - Particle Gun. Επίσης για την αξιολόγηση χρησιμοποιήθηκαν δεδομένα από το πείραμα CMS: αλληλεπιδράσεις πρωτονίων με πρωτόνια και αλληλεπιδράσεις βαρέων ιόντων αλλά και γεγονότα κοσμικής ακτινοβολίας. Στις επόμενες παραγράφους παρουσιάζεται η αξιολόγηση του BMTF.

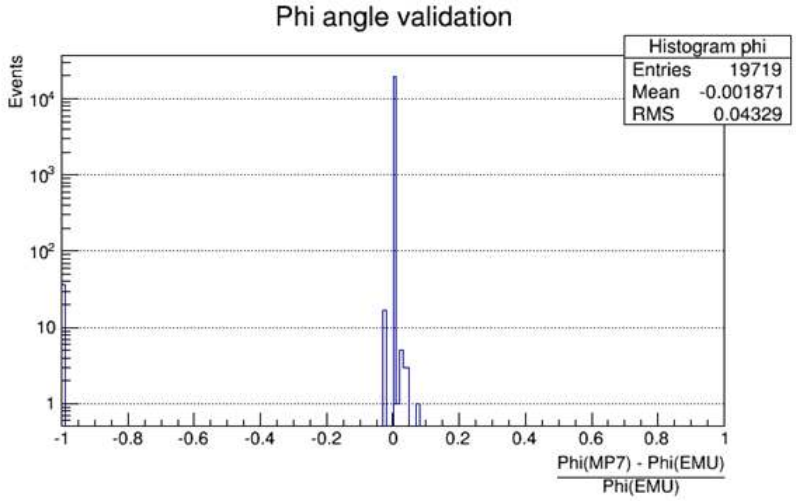
Έλεγχος σωστής λειτουργίας του BMTF με την χρήση δεδομένων προσομοίωσης Monte Carlo

Τα δεδομένα της προσομοίωσης συγκρούσεων πρωτονίων Monte Carlo, αποθηκεύτηκαν σε μνήμες εισόδου της κάρτας MP7. Ο αλγόριθμος της κάρτας βρήκε τις τροχιές των μιονίων από την πληροφορία της εισόδου και τα αποτελέσματα αποθηκεύτηκαν σε μνήμες εξόδου, απ' όπου και ανακτήθηκαν. Τα αποτελέσματα συγκρίθηκαν ένα προς ένα με τα αποτελέσματα της ανάλυσης offline με ανεξάρτητο λογισμικό που χρησιμοποιεί τον αλγόριθμο του BMTF. Η σύγκριση δείχνει τη σωστή ή μη εφαρμογή του αλγόριθμου στο hardware.

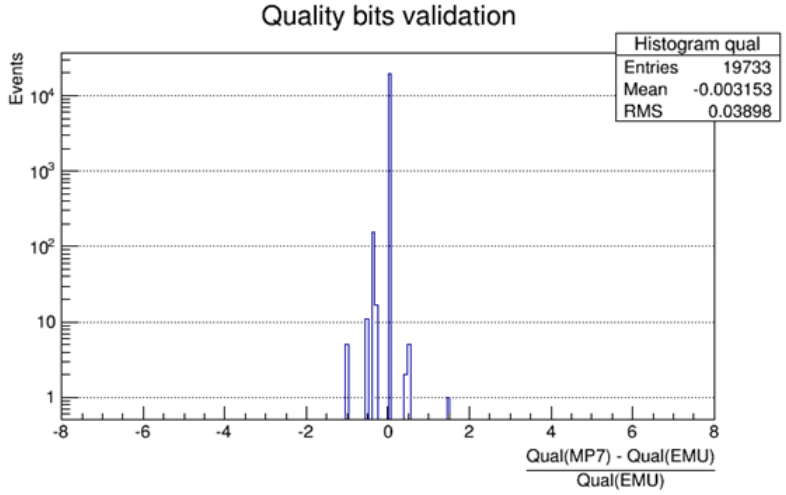


Εικόνα 15: Σύγκριση του p_T της κάρτας MP7 ως προς το p_T του συστήματος απομίμησης.

Το λογισμικό της ανάλυσης offline ονομάζεται σύστημα απομίμησης (emulator) BMTF και εφαρμόζει τους ίδιους αλγόριθμους με αυτούς που υλοποιεί το hardware. Για τον έλεγχο πολλαπλάσιου πλήθους προσομοιωμένων μιονίων από την χωρητικότητα της εσωτερικής μνήμης της κάρτας MP7, χρησιμοποιήθηκε λογισμικό που αναπτύχθηκε σε γλώσσα προγραμματισμού python. Το λογισμικό χρησιμοποιεί ως μέσον αποθήκευσης αρχείο XML (xml parsing). Ο ικανοποιητικός αριθμός γεγονότων με μιόνια (20.000 γεγονότα) βοηθά στον εντοπισμό των διαφορών μεταξύ του αλγόριθμου που υλοποιείται στην κάρτα και του αλγόριθμου που υλοποιείται στο λογισμικό (σύστημα απομίμησης), άρα και στον εντοπισμό των σφαλμάτων.



Εικόνα 16: Σύγκριση του phi της κάρτας MP7 ως προς το phi του συστήματος απομίμησης.



Εικόνα 17: Σύγκριση του quality της κάρτας MP7 ως προς το quality του συστήματος απομίμησης.

Στα ιστογράμματα των σχημάτων 15, 16 και 17 παρουσιάζονται οι κανονικοποιημένες διαφορές των εξόδων από την MP7 της εγκάρσιας ορμής (p_T), της εγκάρσιας γωνίας κλίσης (phi) καθώς και της ποιότητας της τροχιάς (quality bits) ως προς τις αντίστοιχες εξόδους του συστήματος απομίμησης. Ένας μικρός αριθμός από τα μιόνια στα 20.000 γεγονότα δίνει ποσότητα άπειρης τιμής στα ιστογράμματα και γι' αυτό δεν παρουσιάζεται σε αυτά. Ο απειρισμός αυτός οφείλεται στον μηδενισμό του παρονομαστή της τεταγμένης των ιστογραμμάτων (p_T/phi/qual*(EMU)*=0). Τα δεδομένα εισόδου (φυσικές - κινηματικές παράμετροι των μιονίων των 20.000 γεγονότων) παράχθηκαν με λογισμικό προσομοίωσης των αλληλοεπιδράσεων πρωτονίων - πρωτονίων του CMS. Τα μιόνια που δημιουργούνται στο σημείο συγκρούσεων παίρνουν τιμές εγκάρσιας ορμής από 6 GeV έως 1 TeV με βήμα 0.5 GeV. Στα ιστογράμματα το MP7 αντιστοιχεί στην έξοδο της κάρτας και το EMU στην έξοδο του συστήματος απομίμησης του αλγόριθμου. Μετά την σύγκριση της εξόδου του συστήματος απομίμησης με αυτήν της κάρτας MP7, το πλήθος των γεγονότων με διαφορετικές τιμές στα 20.000 μιόνια ήταν: 39 για το p_T, 68 για το phi

και 196 για τα quality bits. Το αποτέλεσμα αποδεικνύει ότι η κάρτα και το σύστημα απομίμησης βρίσκονται σε καλή συμφωνία και άρα ότι ο αλγόριθμος έχει ενσωματωθεί σωστά στις κάρτες του BMTF.

Ενσωμάτωση του BMTF στο L1T - Εγκατάσταση και ρυθμίσεις (Commissioning)

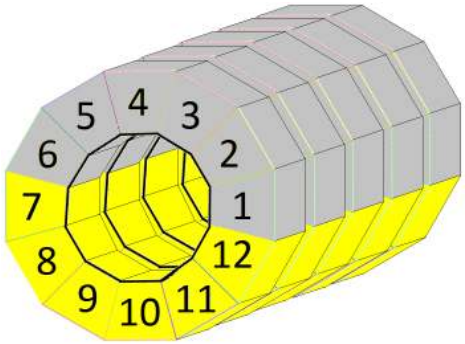
Το σύστημα BMTF εγκαταστάθηκε στο CMS κατά τη διάρκεια της ετήσιας παύσης εργασιών, στις αρχές του 2016. Ενσωματώθηκε ως τμήμα του αναβαθμισμένου συστήματος σκανδαλισμού L1T του πειράματος CMS, το οποίο την περίοδο αυτή βρισκόταν σε κατάσταση εγκατάστασης και ρύθμισης (commissioning). Η είσοδος του BMTF προέρχεται από το σύστημα TwinMux με το οποίο συνδέεται με 360 οπτικές ίνες. Όπως φαίνεται στην εικόνα 18, χρησιμοποιείται πάνελ διασύνδεσης (patch panel), στην εξωτερική πλευρα του οποίου συνδέονται οι οπτικές ίνες των εισόδων του BMTF και στην εσωτερική οι έξοδοι του συστήματος TwinMux. Κατά τον έλεγχο της μετάδοσης των δεδομένων στο BMTF παρουσιάστηκαν ορισμένα προβλήματα, τα οποία αφορούσαν οπτικές ίνες και συστήματα minipods χαμηλής απόδοσης τα οποία αντικαταστάθηκαν. Το BMTF λαμβάνει δεδομένα από όλους τους ανιχνευτές των μιονίων της κεντρικής περιοχής του CMS. Την περίοδο προετοιμασίας όλα τα συστήματα του L1T αναβαθμίστηκαν παράλληλα.

Εικόνα 18: Οπτικές ζεύξεις των εισόδων του συστήματος BMTF

Για την τελική ενσωμάτωση του BMTF έγιναν κατάλληλες τροποποιήσεις στην λογική συλλογής δεδομένων (DAQ) αλλά και στον διαθέσιμο χρόνο για επεξεργασία (latency) μέχρι την παραγωγή του σήματος σκανδαλισμού των μιονίων. Πριν την αναβάθμιση το BMTF χρειαζόταν χρόνο για επεξεργασία ίσο με το χρόνο 33 διαδοχικών αλληλεπιδράσεων των πακέτων πρωτονίων (bunch crossings, BXs). Μετά από βελτιστοποιήσεις της λογικής, η οποία υλοποιήθηκε σε γλώσσα προγραμματισμού VHDL, το latency μειώθηκε στα 14 BXs.

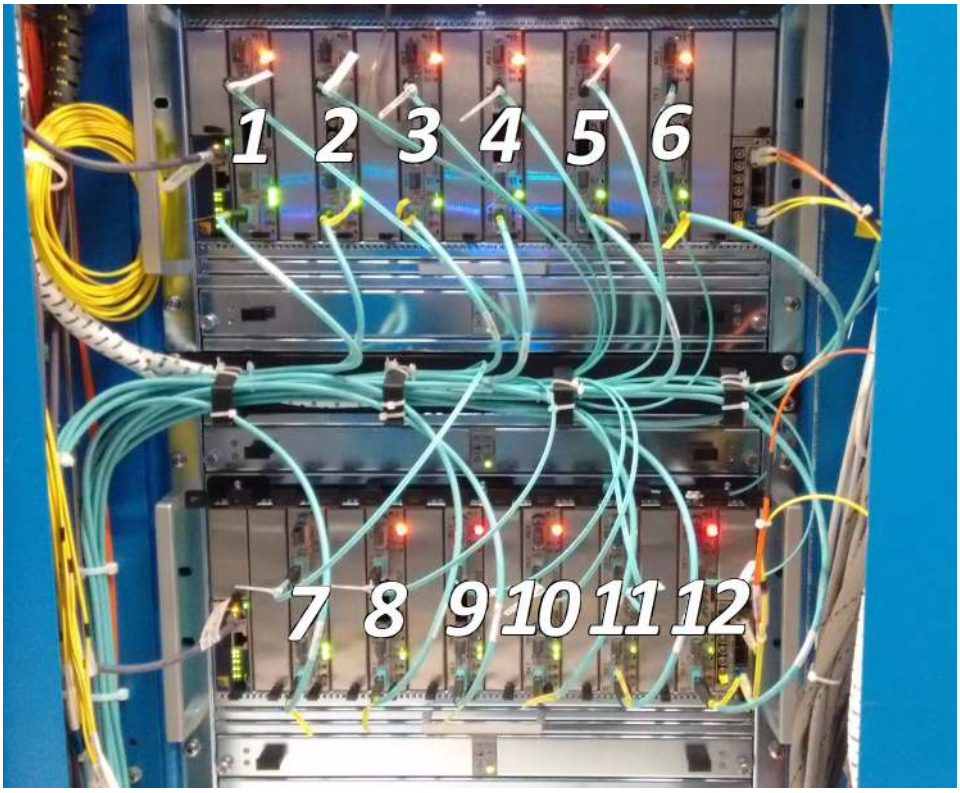
Στην εικόνα 19 παρουσιάζονται οι ομάδες από σφήνες ανιχνευτών DT και RPC που επεξεργάζονται οι ηλεκτρονικές κάρτες του BMTF. Το σύστημα αποτελείται από δύο μέρη, το κάθε ένα εκ των οποίων εξυπηρετεί 6 σφηνοειδή τμήματα. Το άνω τμήμα

εξυπηρετεί τα σφηνοειδή τμήματα 1 έως 6 και το κάτω τμήμα τα σφηνοειδή τμήματα 7 έως 12. Κάθε κάρτα MP7 του BMTF βρίσκει τροχιές ενός σφηνοειδούς τμήματος.



Εικόνα 19: Τα δώδεκα wedges ανιχνευτών που εξυπηρετεί ο BMTF.

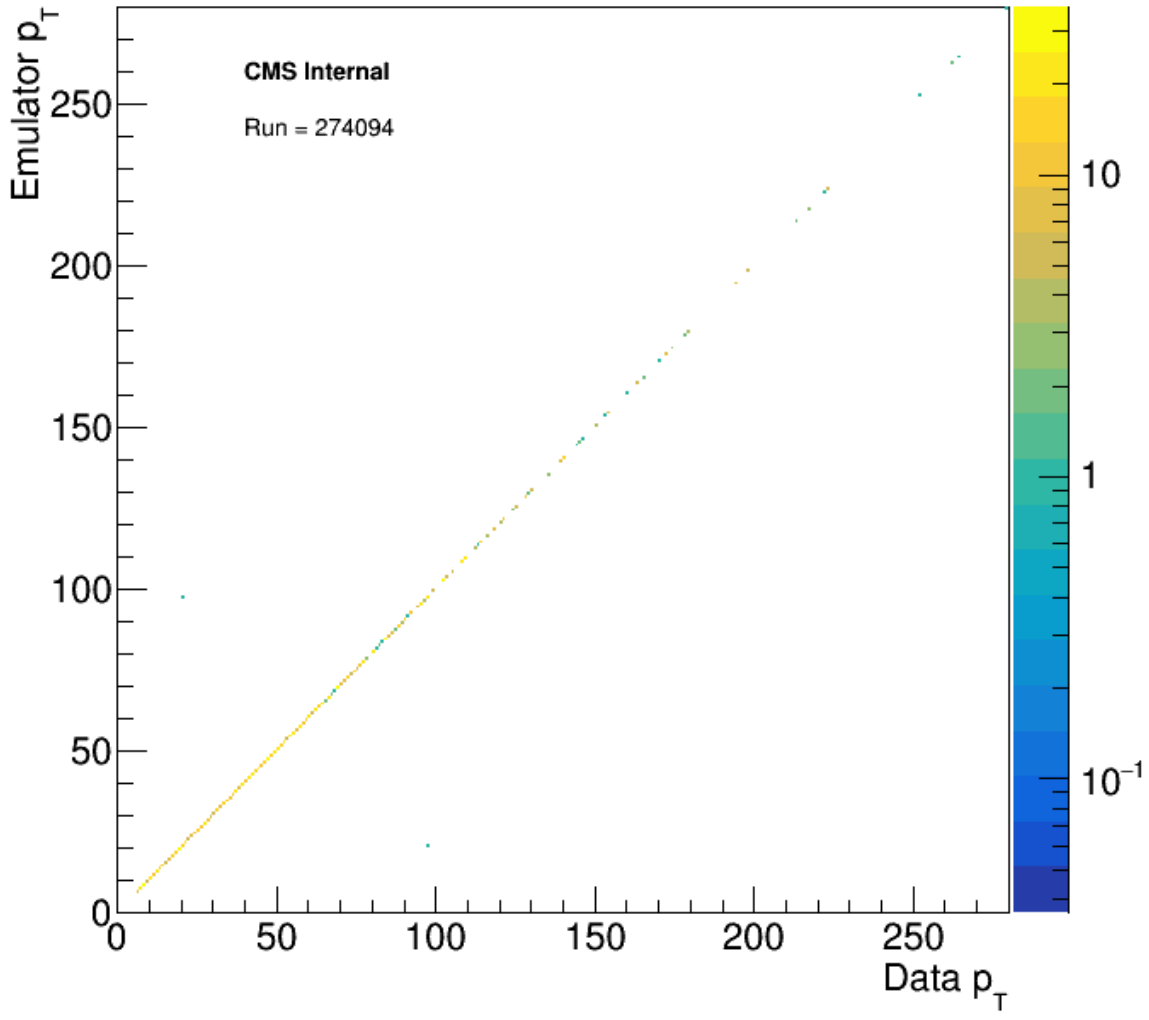
Στην εικόνα 20 παρουσιάζεται το σύστημα BMTF εγκατεστημένο. Το πάνω τμήμα του BMTF χρησιμοποιεί το πάνω πλαίσιο μTCA και αντίστοιχα το κάτω εξυπηρετείται από το κάτω πλαίσιο μTCA. Και τα δύο τμήματα χρησιμοποιούν 6 επεξεργαστές MP7, 1 κάρτα συλλογής και μορφοποίησης των δεδομένων AMC13 και 1 κάρτα ελέγχου του πλαισίου MCH. Στην εικόνα 13 φαίνονται επίσης και οι οπτικές ίνες που συνδέονται στις κάρτες MP7.



Εικόνα 20: Το σύστημα σκανδαλισμού BMTF.

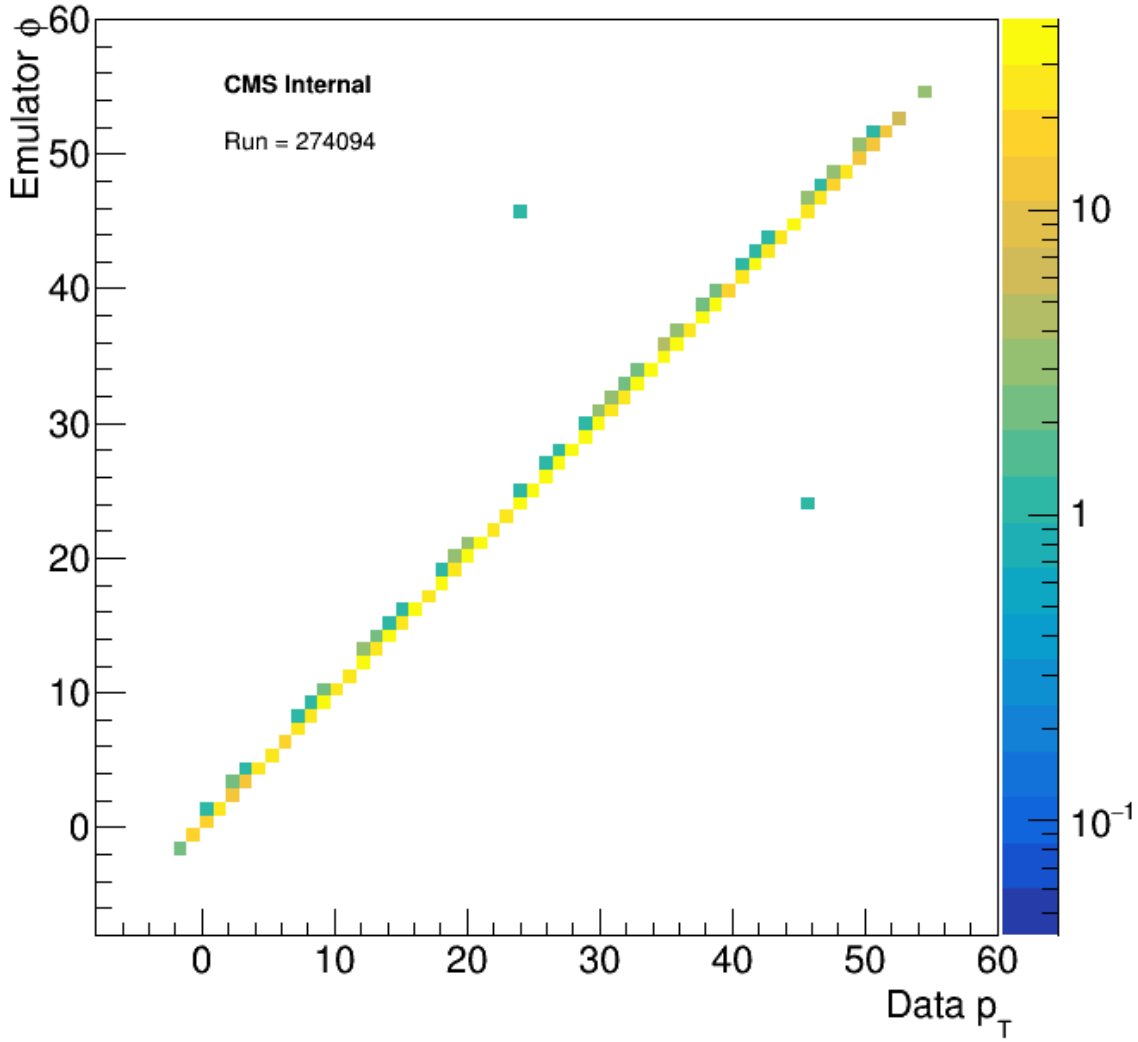
Έλεγχος λειτουργίας του συστήματος BMTF μέσω αλληλεπιδράσεων πρωτονίων στο CMS

Μετά από την ενσωμάτωση του BMTF στο γενικό σύστημα σκανδαλισμού L1T, τα αποτελέσματά του στέλνονται στο μGMT και αποθηκεύονται σε μνήμη τύπου First−in First−out (FiFo). Ο χρόνος αποθήκευσης είναι ίσος με το άθροισμα του χρόνου που χρειάζεται το υπόλοιπο L1T να επεξεργαστεί τα αποτελέσματα του BMTF και να παράξει το σήμα Level-1 accept (L1A) και του χρόνου που απαιτείται να φτάσει το σήμα L1T από το μGT πίσω στο BMTF μέσω του συστήματος χρονισμού του συστήματος σκανδαλισμού (TCDS). Τότε και εφ' όσον έχει πραγματοποιηθεί σκανδαλισμός L1A, το BMTF στέλνει τα δεδομένα του στο σύστημα συλλογής δεδομένων DAQ. Τα δεδομένα αυτά χρησιμοποιούνται στην ανάλυση. Τα δεδομένα της εισόδου του BMTF χρησιμοποιούνται και στο σύστημα απομίμησης, η έξοδος του οποίου συγκρίνεται με την έξοδο του BMTF.



Εικόνα 21: Συγκρίσεις μεταξύ των δεδομένων p_T εξόδου του BMTF με τα αποτελέσματα του συστήματος απομίμησης.

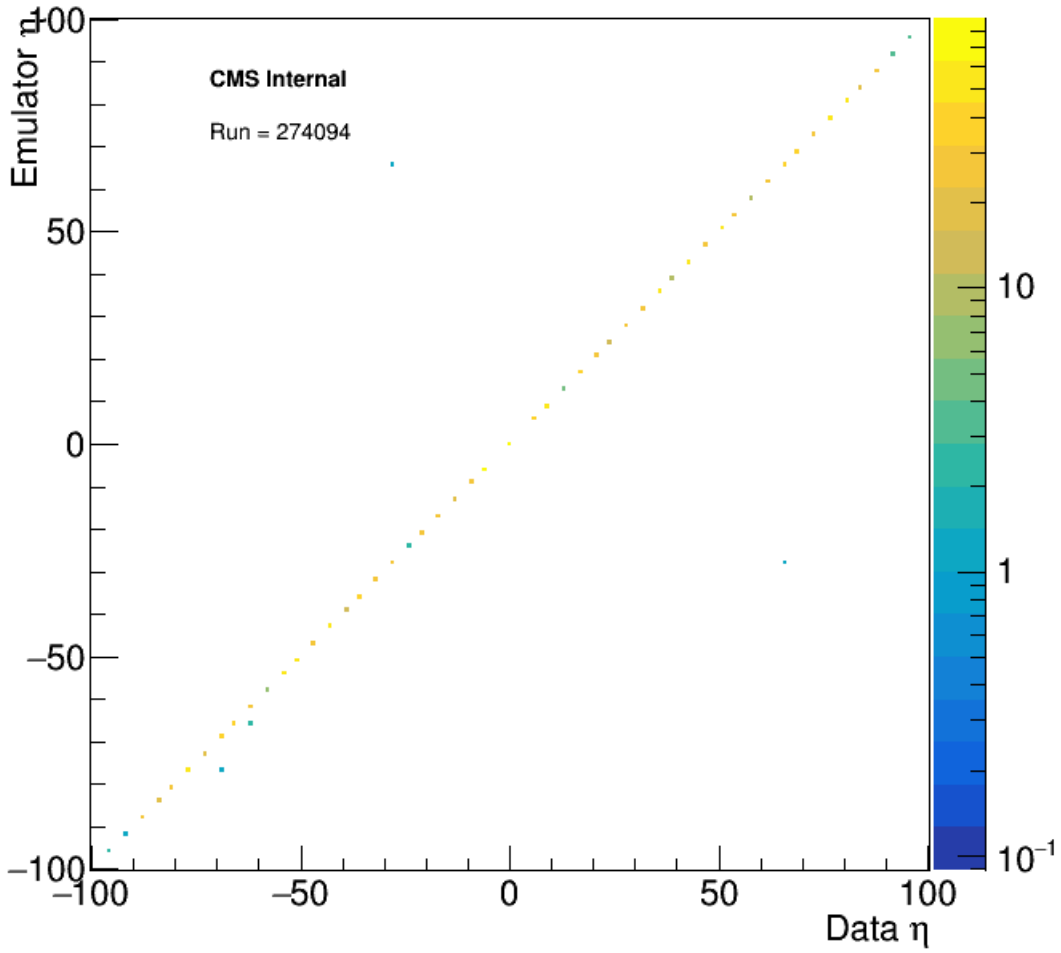
Κατά την λειτουργία (Run274094) του CMS καταγράφηκαν δεδομένα της εισόδου και της εξόδου του BMTF από αλληλεπιδράσεις πρωτονίων. Τα δεδομένα συλλέχθηκαν με σκοπό την σύγκριση των δεδομένων εξόδου του υλικού BMTF με τα δεδομένα που παράγει το σύστημα απομίμησης των αλγορίθμων για τα ίδια δεδομένα εισόδου υπό κανονικές συνθήκες λειτουργίας. Στην εικόνα 21 φαίνονται τα αποτελέσματα των συγκρίσεων του μεγέθους της εγκάρσιας ορμής (p_T) του υλικού BMTF με αυτήν του συστήματος απομίμησης. Στην τετμημένη βρίσκεται ο άξονας των τιμών p_T που συλλέχθηκαν από την κάρτα (Data p_T) και στην τεταγμένη βρίσκεται ο άξονας των τιμών p_T που παρήγαγε το σύστημα απομίμησης των αλγορίθμων (Emulator p_T).



Εικόνα 22: Συγκρίσεις μεταξύ των δεδομένων ϕ εξόδου του BMTF με τα αποτελέσματα του συστήματος απομίμησης.

Η τρίτη διάσταση της εικόνας 21, παρουσιάζεται με χρώματα της παλέτας στα δεξιά. Το χρώμα υποδηλώνει το πλήθος των μετρήσεων για κάθε p_T bin. Σχεδόν όλα τα αποτελέσματα βρίσκονται πάνω στην διαγώνιο αποδεικνύοντας ότι το σύστημα BMTF και το σύστημα απομίμησης των αλγορίθμων παρουσιάζουν καλή συμφωνία μεταξύ

τους και άρα ότι το υλικό και η εφαρμοσμένη λογική στο σύστημα BMTF λειτουργούν ικανοποιητικά.



Εικόνα 23: Συγκρίσεις μεταξύ των δεδομένων ϕ εξόδου του BMTF με τα αποτελέσματα του συστήματος απομίμησης.

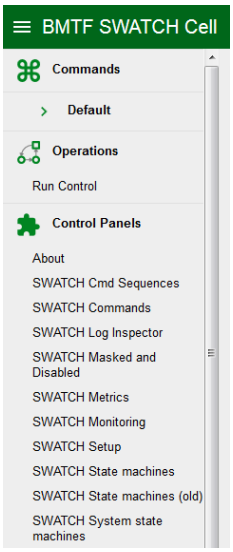
Συγκρίσεις των μεγεθών ϕ και η του συστήματος BMTF με το σύστημα απομίμησης των αλγορίθμων, αντίστοιχες με αυτές του μεγέθους της p_T, παρουσιάζονται στις εικόνες 22 και 23. Όπως και στην εικόνα 21, στις 22 και 23 παρουσιάζεται η καλή συμφωνία του συστήματος BMTF με το σύστημα απομίμησης των αλγορίθμων και άρα ο αλγόριθμος που εφαρμόστηκε στις κάρτες MP7, υλοποιήθηκε σωστά.

Το πλήθος των διαφορών που βρέθηκαν από συνολικά 9.177 μιόνια βρίσκονται εκτός της διαγωνίου των εικόνων 21, 22 και 23. Όπως φαίνεται στην εικόνα 16, οι περισσότερες διαφορές ϕ μεταξύ του υλοποιημένου συστήματος στις κάρτες MP7 και στο σύστημα απομίμησης που βρέθηκαν διαφέρουν κατά μία μονάδα, το οποίο θεωρείται αμελητέα ποσότητα διότι δεν επηρεάζει τα αποτελέσματα των επόμενων βαθμίδων σκανδαλισμού. Οι ποσότητες p_T, ϕ και η παρουσιάζουν ελάχιστες διαφορές, το πλήθος των οποίων φαίνεται στον πίνακα 1. Οι διαφορές αυτές οφείλονται σε μικρά σφάλματα που δημιουργήθηκαν κατά την ανάπτυξη του κώδικα VHDL.

	Πλήθος διαφορών	Ποσοστό συμφωνίας
p_T	19	99.79%
ϕ	232	97.47%
η	14	99.85%

Πίνακας 1: Διαφορές των φυσικών μεγεθών μεταξύ του υλοποιημένου συστήματος σε κάρτες MP7 και του συστήματος απομίμησης.

Σύστημα ελέγχου του BMTF από το κέντρο γενικού ελέγχου



Εικόνα 24: Κέλυφος BMTF

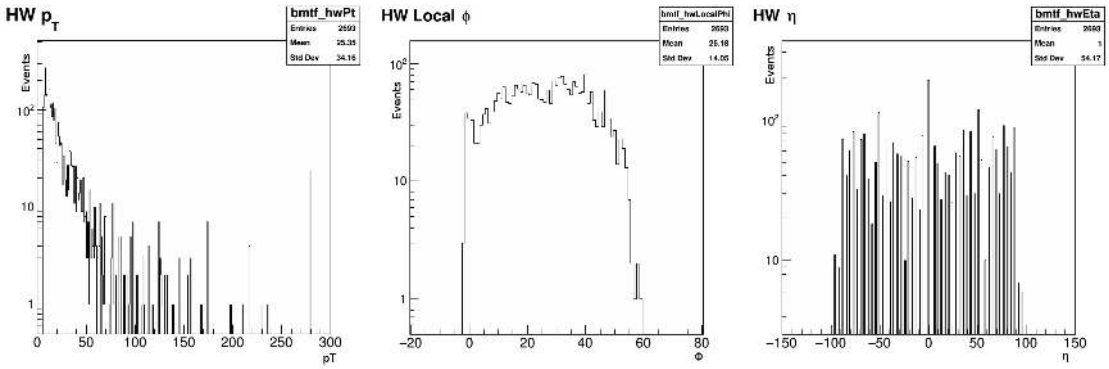
Το σύστημα BMTF όπως και όλα τα συστήματα L1T του CMS ελέγχονται από λογισμικό που χρησιμοποιεί μία πλατφόρμα ελέγχου για κάθε σύστημα σκανδαλισμού που ονομάζεται SWATCH (SoftWare for Automating conTrol Common Hardware) [6]. Το SWATCH για την επικοινωνία του με τις ηλεκτρονικές μονάδες χρησιμοποιεί την διεπαφή IPbus [7]. Στην εικόνα 24 φαίνεται η διεπαφή χρήσης του SWATCH του BMTF, με τα πάνελ ελέγχου (Control Panels). Μέσω της επιλογής Commands ο χρήστης μπορεί να δώσει βασικές εντολές (halt, configure, start), ενώ από το SWATCH Setup μπορεί να αλλάξει τις παραμέτρους του συστήματος όπως συχνότητα δειγματοληψίας της συχνότητας σκανδαλισμού και απενεργοποίηση τμημάτων του αλγόριθμου. Μέσω των επιλογών του SWATCH masked and Disabled μπορούν να απενεργοποιηθούν οπτικές σειριακές είσοδοι (optical links) του συστήματος που τυχόν παράγουν θόρυβο και μέσω της SWATCH State machines μπορούν να τροποποιηθούν βασικές λειτουργίες σε κάθε ηλεκτρονική κάρτα. Επιπλέον μέσω του SWATCH Monitoring και του SWATCH Metrics ο χρήστης μπορεί να ελέγξει την απόδοση του BMTF. Στην εικόνα 24 παρουσιάζεται το αντίστοιχο γράφημα με τις συχνότητες σκανδαλισμού της εξόδου για κάθε μία από τις 12 κάρτες του BMTF.

Εικόνα 25: Διάγραμμα μεταβολής της συχνότητας σκανδαλισμού του BMTF ως προς τον χρόνο από το SWATCH.

Παρατηρείται ότι οι 12 επεξεργαστές του συστήματος BMTF παρουσιάζουν σχεδόν σταθερή μείωση συχνότητας σκανδαλισμού (ακολουθώντας την μείωση της στιγμιαίας φωτεινότητας στο πείραμα) με εξαίρεση ορισμένες πτώσεις, που δημιουργούνται λόγω της σύντομης απώλειας της φωτεινότητας της δέσμης, η οποία συμβαίνει στο CMS όταν γίνεται σάρωση της δέσμης πρωτονίων (beam scanning) για λόγους ευθυγράμμισης της δέσμης. Δηλαδή, φαίνεται ότι δεν υπάρχουν διακυμάνσεις οι οποίες να παραπέμπουν σε θόρυβο στην είσοδο του συστήματος ή σε κάποια διαταραχή του.

Σύστημα ελέγχου ποιότητας των δεδομένων Data Quality Monitoring (online DQM)

Κατά την λειτουργία του συστήματος BMTF αποστέλλονται μέσω του συστήματος DAQ προς το λογισμικό ελέγχου (online DAQ) οι είσοδοι και οι αντίστοιχες έξοδοι του συστήματος. Τα δεδομένα παρουσιάζονται σε ιστογράμματα από το λογισμικό ελέγχου. Στην εικόνα 25 παρουσιάζονται ιστογράμματα των p_T, ϕ και η του BMTF. Τα ιστογράμματα αυτά ανανεώνονται όταν το σύστημα σκανδαλισμού βρίσκεται σε λειτουργία. Έτσι ο χρήστης ελέγχει αν το σύστημα παρουσιάζει ομαλή λειτουργία σε συνάρτηση με το χρόνο.



Εικόνα 26: Online DQM: p_T (αριστερά), ϕ (μέση) και η (δεξιά).

Ανακεφαλαίωση – Σχόλια

Η ανάπτυξη του συστήματος BMTF, που περιγράφεται στην παρούσα διδακτορική διατριβή, χρησιμοποιήθηκε στο πρώτο επίπεδο σκανδαλισμού του πειράματος CMS. Το ηλεκτρονικό σχέδιο του συστήματος σε VHDL φορτώνεται στις ηλεκτρονικές κάρτες MP7 με τις κατάλληλες παραμέτρους. Το σύστημα BMTF αν βρει τροχιές μιονίων στέλνει τα αποτελέσματα στο σύστημα Data Acquisition (DAQ) από όπου τελικά παρουσιάζονται στο σήμα ελέγχου SWATCH. Το λογισμικό επιτηρεί το σύστημα και παρέχει στον χρήστη εργαλεία για να εκτιμήσει αν το σύστημα λειτουργεί ικανοποιητικά.

Η αναβάθμιση του συστήματος εύρεσης μιονίων της κεντρικής περιοχής (BMTF) έχει ως αποτέλεσμα την μείωση του ρυθμού σκανδαλισμού του νέου συστήματος σε σχέση με το παλιό κατά περίπου 40% και την σχεδόν ίδια αποδοτικότητα του στην εύρεση μιονίων.

Η αναβάθμιση αυτή εισήγαγε μια μοντέρνα τεχνολογία στο σύστημα σκανδαλισμού του CMS, η οποία συμβάλλει στην σταθερότητα του συστήματος και εξασφαλίζει την

διατήρηση του υλικού για τα επόμενα χρόνια, έτσι ώστε έως την επόμενη φάση της αναβάθμισης CMS upgrade phase II που θα γίνει την περίοδο 2023-2025 να αλλάζει μόνο η λογική, δηλαδή το φορτωμένο ηλεκτρονικό σχέδιο του συστήματος γραμμένο σε VHDL (firmware), και όχι το υλικό.

Αναφορές

[1] S. Dasu et al. CMS. The TriDAS project. Technical design report, vol. 1: The trigger systems. 2000.

[2] A Tapper and Darin Acosta. CMS Technical Design Report for the Level-1 Trigger Upgrade. Technical Report CERN-LHCC-2013-011. CMS-TDR-12, CERN, Geneva, Jun 2013. Additional contacts: Jeffrey Spalding, Fermilab, Jeffrey.Spalding@cern.ch Didier Contardo, Universite Claude Bernard-Lyon I, didier.claude.contardo@cern.ch.

[3] G. Iles, J. Jones, and A. Rose. Experience powering Xilinx Virtex-7 FPGAs. JINST, 8:C12037, 2013.

[4] Andrea Triossi, Marco Bellato, Roberto Isocrate, Fabio Montecassiano, and Sandro Ventura. A New Data Concentrator for the CMS Muon Barrel Track Finder. PoS, TIPP2014:412, 2014.

[5] S. Chatrchyan et al. The CMS experiment at the CERN LHC. JINST, 3:S08004, 2008.

[6] Jim Brooke, Karol Bunkowski, Ivan Cali, Carlos Ghabrous Larrea, Christos Lazaridis, and Alessandro Thea. SWATCH: common control SW for the uTCA-based upgraded CMS L1 Trigger. J. Phys.: Conf. Ser., 664(8):082012. 8p, 2015.

[7] C. Ghabrous Larrea, K. Harder, D. Newbold, D. Sankey, A. Rose, A. Thea, and T. Williams. Ipbus: a flexible ethernet-based control system for xtca hardware. Journal of Instrumentation, 10(02):C02019, 2015.

Part II

The CMS Level-1 Trigger Upgrade – Barrel Muon Track Finder

Chapter 1

Introduction

The idea that matter consists of smaller particles and that there exists a limited number of primary, elementary particles in nature has existed in natural philosophy at least since the 5th century BC. In ancient Greece, Democritus and his mentor Leucippus introduced the theory of Atomism. The atomists theorized that nature consists of two fundamental quantities: atom and void. According to this philosophy the atoms are physically, but not geometrically, indivisible, have always been and always will be in motion and between them lies empty space.

According to the current understanding, nature is made of particles which are also indivisible. The branch of physics which studies elementary particles and their properties is called particle physics. There are three categories of elementary particles which are the fundamental constituents of all objects in Universe. Quarks, leptons and bosons. They use four fundamental forces to interact with each other: the electromagnetic, the strong and weak nuclear interactions and gravity. The strong interaction is responsible for holding quarks together to form hadrons and also holding neutrons and protons together to form atomic nuclei. In the strong interaction, the exchange of gluon particles mediate the force. The electromagnetic interaction acts on electrically charged particles through the exchange of photons. The weak interaction is a short-range interaction responsible for some forms of radioactivity, and acts on leptons and quarks. The mediators of the week interactions are the W and Z bosons. Finally, the gravitational interaction is a long-range attractive one that acts on all massive particles, probably through the exchange of a graviton. The modern unified field theory attempts to bring these four interactions together into a single framework.

1.1 The Standard Model

The Standard Model (SM) is one of the great triumphs of modern day physics, successfully explaining many aspects of ElectroWeak (EW) and strong interactions, confirmed through decades of precise experimental data. After the announcement in July 2012 of the discovery of a particle whose properties are consistent with those of a Higgs boson [8, 9], the long-awaited missing link of the SM, one could suggest that the SM picture is complete. However, despite the incredible achievements of the theory, there are several observed phenomena that cannot be explained by the SM. In fact, the SM is expected to be an *effective theory*, valid up to some cutoff

scale Λ. The Large Hadron Collider (LHC) was built in order to probe the validity of the SM and look for solutions to some of the unknown issues in particle physics that may involve physics beyond the SM.

The Standard Model is a formulation in terms of gauge theories of three of the four fundamental forces of nature – the strong, weak and electromagnetic interactions. The strong interaction, or strong nuclear force, is the most complicated interaction, mainly because of the way it varies with distance. Moreover, it holds inside hadrons and also during the showering and fragmentation of jets and as a result is responsible for the majority of hadrons properties. It strong interaction is described by Quantum Chromodynamics (QCD). QCD is a theory of fractionally charged fermions (quarks) interacting by means of eight photon-like particles called gluons. On the other hand, the weak force is responsible for some nuclear phenomena such as beta decay. Electromagnetism and the weak force are now understood to be two aspects of a unified ElectroWeak interaction (EW) – this discovery was the first step toward a unified Standard Model. In the theory of the electroweak interaction, the carriers of the weak force are the massive gauge bosons called the W and Z bosons. Finally, electromagnetism is the force that acts between electrically charged particles. This infinite-ranged interaction is described precisely by the theory of Quantum Electrodynamics (QED). Some details of the fundamental interactions of nature are collected in Table 1.1. The interaction of Gravity is by far the weakest of the four interactions and it is not described on the framework of the Standard Model.

Interaction	Theory	Mediator	Relative Strength
Strong	QCD	gluons (g)	10^{38}
Electromagnetic	QED	photon (γ)	10^{35}
Weak	Electroweak Theory	$W^{\pm}$ and Z^0	10^{25}
Gravitation	General Relativity	graviton (hypothetical)	1

Table 1.1: The four fundamental interactions of nature with the corresponding mediators, the current theoretical model of description and the relevant strength. Graviton is an hypothetical spin-2 particle.

The formalism of the SM is based on the non-Abelian gauge group

$$SU(3)_c \times SU(2)_L \times U(1)_Y,$$

where $SU(3)_c$ is the gauge group of Quantum Chromodynamics (QCD) and $SU(2)_L \times U(1)_Y$ is the gauge group of the Electroweak theory. Particles are classified according to their transformations under these symmetry groups, as well as being grouped into two categories based on their spin fermions possessing half-odd-integer spins, and bosons possessing integer spins. The fermions of the SM transform in a spin $\frac{1}{2}$ representation of the Lorentz group and interact with each other by exchanging spin 1 vector bosons, while the only Lorentz scalar of the SM is the Higgs boson which is responsible for generating mass for the other particles.

The SM is a chiral theory with left-handed fermions transforming as doublets of $SU(2)_L$ and right-handed fermions transforming as singlets of this group. Associated

with $SU(2)_L$ are three gauge bosons, W^+, W^- and Z^0, which mediate weak interactions and whose mass is responsible for the short range of the weak force. The electroweak group is broken at low energies to $U(1)_{EM}$, called gauge group of electromagnetism. This force is mediated by the massless photon (γ). Applying the principles of gauge theory to QCD leads to the notion of colour, where quarks can be "blue", "green" or "red" and gauge transformations are local transformations between quarks of different colours. The gauge bosons of QCD which mediate the strong interactions are called gluons (g), and together with the gauge bosons of the electroweak theory complete the "force carriers" of the SM. The Table 1.2 below presents the particle content of the SM with details about the spin and the electric charge of each field.

Type	Particles			Spin	Charge
Leptons	$\begin{pmatrix} \nu_e \\ e^- \end{pmatrix}_L$	$\begin{pmatrix} \nu_\mu \\ \mu^- \end{pmatrix}_L$	$\begin{pmatrix} \nu_\tau \\ \tau^- \end{pmatrix}_L$	$\begin{pmatrix} 1/2 \\ 1/2 \end{pmatrix}$	$\begin{matrix} 0 \\ -1 \end{matrix}$
	e_R^-	μ_R^-	τ_R^-	$1/2$	-1
Quarks	$\begin{pmatrix} u \\ d \end{pmatrix}_L$	$\begin{pmatrix} c \\ s \end{pmatrix}_L$	$\begin{pmatrix} t \\ b \end{pmatrix}_L$	$\begin{pmatrix} 1/2 \\ 1/2 \end{pmatrix}$	$\begin{matrix} +2/3 \\ -1/3 \end{matrix}$
	u_R	c_R	t_R	$1/2$	$+2/3$
	d_R	s_R	b_R	$1/2$	$-1/3$
Vector Bosons	γ			1	0
	$W^\pm$ and Z			1	± 1 and 0
	g			1	0
Scalar Bosons	H			0	0

Table 1.2: The particle content of the Standard Model with the corresponding spin and charges.

As we can see from the Table, the fermionic matter content of the SM can be divided into three generations, with each member of a generation having greater mass than those of lower generations. Each generation is comprised of 1 left-handed lepton doublet $(\nu_e, e^-)_L$, 1-right handed lepton e_R, 3 left-handed quark doublets $(u, d)_L$, 3 right-handed up type quarks u_R and 3 right-handed down type quarks d_R (the factors of 3 for quarks coming from the existence of 3 colours).

1.2 The Large Hadronic Collider at CERN

The European Organization for Nuclear Research or as it is widely know, CERN (Conseil Européen pour la Recherche Nucléaire) is based near Geneva and extends in both France and Switzerland. It was founded in 1954 just after the end of world war II, in order to rekindle European science, foster collaboration between European nations, and study the properties of subatomic particles and the fundamental forces that they obey.

At the Large Hadron Collider (Figure 1.1) large-scale detectors are used for the research of the fundamental aspects of matter at the sub-nuclei level. The accelerated

particles collide in the center of the detectors and the produced particles are detected and analyzed. Electronics digitize the information and generate primitive data. After the processing of the raw data the information is stored and used in the offline analysis. Many physicists, engineers and highly-qualified technicians collaborate in order to develop, upgrade and maintain the experiments.

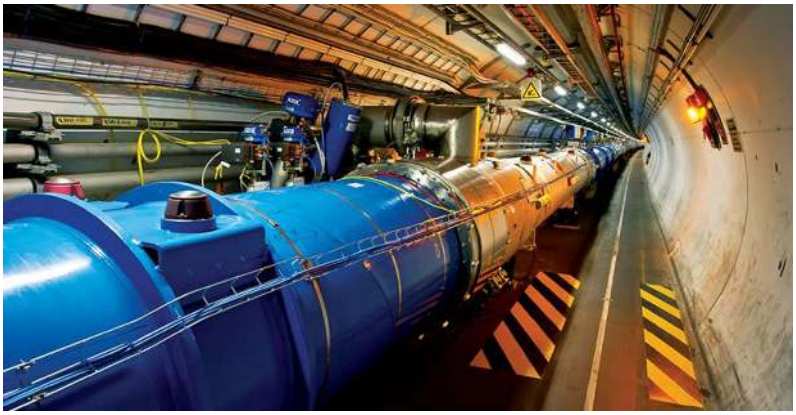


Figure 1.1: LHC tunnel

ATLAS (A Toroidal LHC ApparatuS) and CMS (Compact Muon Solenoid) are general-purpose experiments at LHC searching for same phenomena in order to cross-confirm any new discoveries. ALICE (A Large Ion Collider Experiment) and LHCb (Large Hadron Collider beauty) have detectors specialized on specific phenomena (b-physics, heavy-ion studies). These four detectors are located 100 meters underground in huge caverns in the LHC ring. The smallest experiments on the LHC are TOTEM and LHCf, which focus on particles captured in the forward area of the experiments. MoEDAL uses detectors deployed near LHCb to search for a hypothetical particle called the magnetic monopole.

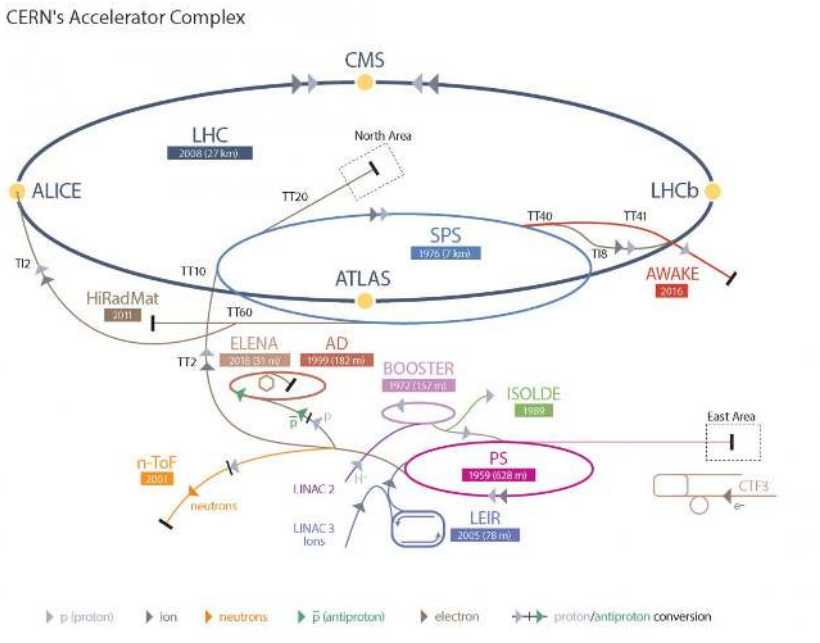


Figure 1.2: Accelerating beam step by step

The first step before the accelerating procedure starts, is to create proton bunches. There come from a simple bottle of hydrogen gas from which an electric field is used to separate hydrogen molecules (H_2) of their electrons to yield protons. As shown in Figure 1.2, the low-energy proton beam is accelerated in the LINear ACcelerator (LINAC2) up to 50 MeV. After that the protons are injected from LINAC2 into a circular accelerator, 157 meters long, called Proton Synchrotron Booster (PSB) which accelerates the proton up to 1.4 GeV. The beam is then delivered to the 628 meter long Proton Synchrotron (PS), where it is accelerated up to 25 GeV. Protons are then sent to the Super Proton Synchrotron (SPS), an underground 6.9-km-long accelerator, where they are accelerated to 450 GeV. They are finally transferred to the LHC in both clockwise and anticlockwise directions, where protons are accelerated to 7 TeV. The LHC is also used to accelerate heavy ions (Pb) at a center of mass energy of 2.76 TeV per ion. Inside the LHC, protons are formed into bunches of $1.15 \text{x} 10^{11}$ protons. The bunch radius at interaction point is 16.7 μm, and its length is 7.55 cm. The distance between two consecutive bunches is 7.48 m, thus in the 26.659 km orbit there is a space for the 3,564 bunches. The Figure 1.3 shows the LHC proton bunches which are grouped in 39 trains, 72 bunches each. The orbit contains only 2,808 bunches of the protons, grouped in trains because the beam structure is determined by the injection scheme and properties of the dump system. The beam orbit in the LHC has missing bunches which are called gaps. In the end of the orbit there is the largest part with proton gaps. This period is called orbit gap and is used by the subsystems to send their status, and reinitiate the optical connections by receiving commas and run Cyclic Redundancy Checks (CRCs).

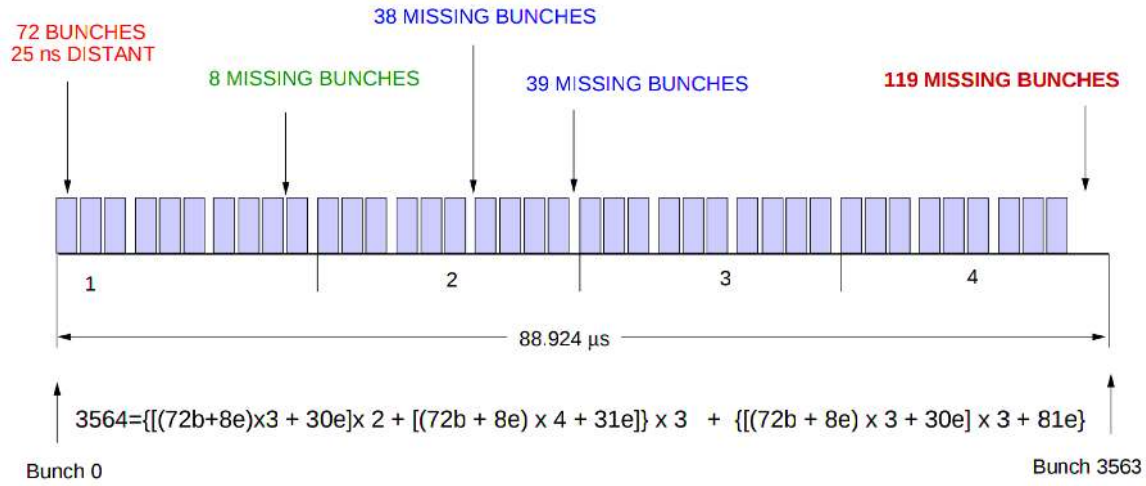


Figure 1.3: The orbit period with the 3,564 bunches in LHC. b and e indicate filled and empty bunches respectively.

The distance between the bunches (7.48 m) divided by the bunch velocity with β = 0.999999991 (relatively velocity of the speed of light), defines the time between the collisions, which is 24.95 ns, which corresponds to the rate of bunch crossing of 40.08 MHz. In every bunch crossing about 20 inelastic proton-proton interactions occur, in most of which unstable particles are produced, which then decay to stable or relatively long-lived objects like electrons, photons, hadron jets, muons and neutrinos. With the exception of neutrinos, these objects are detectable: when they pass the detectors surrounding the interaction point, their properties (direction, energy/momentum,

charge, type) are measured. The complex analysis of the recorded data allows for the reconstruction of the events and, using advanced statistical methods, for the extraction of signals of known or novel physical processes. The high rate of the interactions, as well as the high number and high energy of the produced particles are the major challenges that the LHC detectors have to face [10].

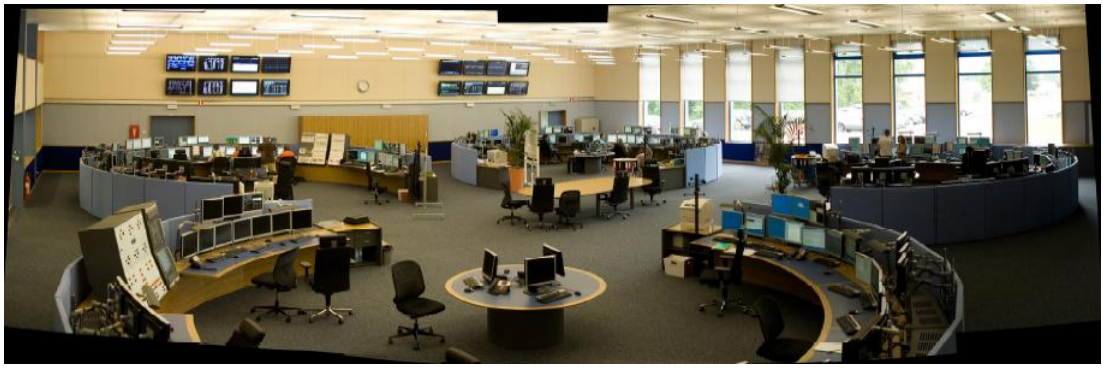


Figure 1.4: CERN Control Center (CCC)

To deliver a good quality of colliding proton bunches, to the LHC experiments, a large and complex control of all accelerators before the LHC is needed. The LHC as well as LINAC2, PSB, PS and SPS are controlled from the CERN Conrtol Center (CCC). The CCC (shown in Figure 1.4) is located in Prevessin side of CERN and has the main control of all experiments. In order to make schedule and deliver the proton bunches with accurate timing and agreed luminosity in LHC, CCC is collaborating with ATLAS, CMS, ALICE and LHCb control rooms. The CMS control room is showing in Figure 1.5.

Figure 1.5: The CMS control room

Chapter 2

The CMS Detector

The detector of the CMS experiment follows a cylindrical geometry and contains several layers of diferent type subdetectors surrounding the interaction point. As shown in Figure 2.1 the inner silicon trackers (TK), the electromagnetic and hadron calorimeters (ECAL and HCAL) and the muon system are the main layers of the CMS detector. One of the most important elements of the detector is the superconducting solenoid, which is the source of the inner uniform magnetic field which provides the measurement of the charged particles through the bending of their trajectories due to the Loentz force. Both ECAL and HCAL as well as TK are inside of the solenoid [11].

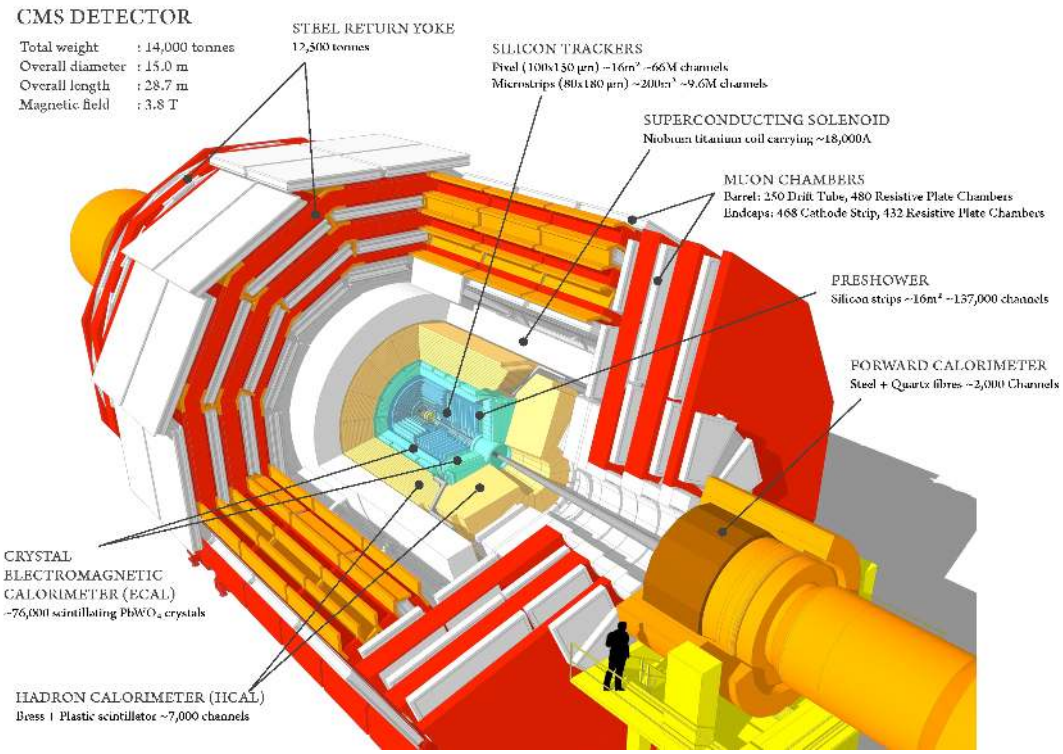


Figure 2.1: The CMS detector

Figure 2.2 shows the two CMS caverns, the CMS detector UXC55 cavern and the data-processing USC55 cavern. The caverns are placed 100 meters underground. One of the LHC interaction points is located in the center of cavern UXC55. Due to

radiation caused by particle passes and beam losses, the detectors and electronics located in UXC55 should be radiation hard. However, it would be difficult and expensive to build the entire experiment electronics according to the radiation hard or tolerant specifications. Therefore, the electronics in UXC55 are limited and their outputs are transmitted and processed in the second cavern, called counting room (USC55). Between the two caverns there is a 7.3-meter-thick concrete wall protecting the counting room from radiation. The USC55 hosts the CMS electronics for trigger and data acquisition. In addition, it hosts the slow-control electronics and CPU. Signal cable, mostly optical fibers of maximum length of 120 m, used for electronic communication between the two caverns.

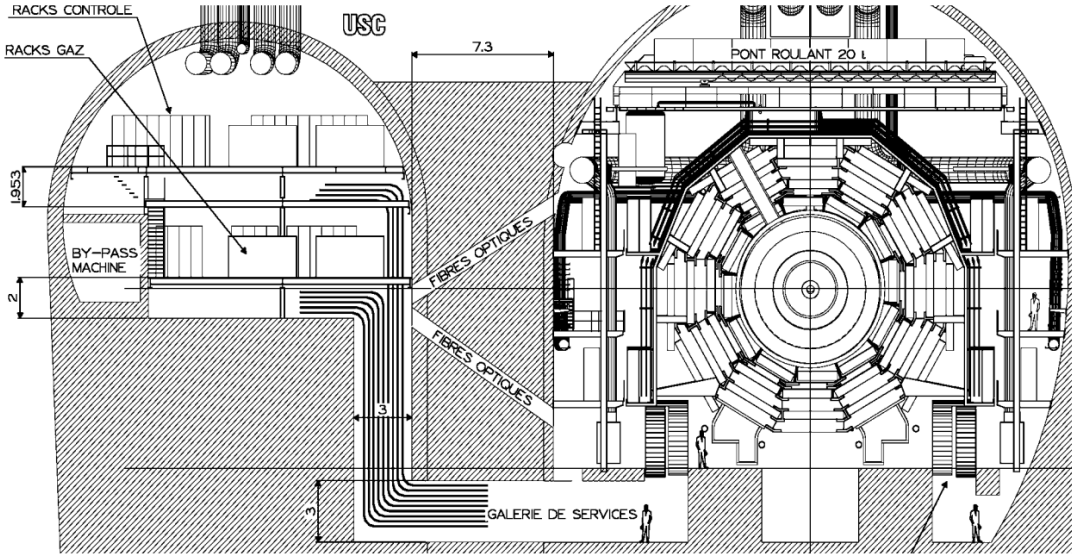


Figure 2.2: CMS caverns. USC55 on the left and UXC55 on the right

The secondary stable or long-leaved particles from the p-p interactions travel though the detector and their passage produce electrical signals. Photons go strait in the ECAL and there leave all their energy. Electrons bend and leave traces while passing through the tracker and then they mostly stop in the ECAL. Charged hadrons (e.g. pions) leave traces in the tracker, pass by ECAL and mostly stop in the HCAL. Neutral hadrons (e.g. neutrons) follow a strait trajectory, they do not interact until they find HCAL where they mostly leave all their energy. Finally, muons bend by the magnetic field and pass through all the layers while they leave traces in the TK and the outer part of the detector where the muon chambers are. The mentioned particles leave critical information at the detectors which is used later by the trigger and offline systems to reconstruct trajectories and calculate the physical parameters of the particles.

The CMS coordinate system has the its origin at the collision point in the center of the detector. In the Cartesian axis system, y-axis is pointing vertically upward toward the surface and the x-axis is pointing radially inward toward the center of LHC. The third dimension , z-axis points along the beam direction toward the Jura mountains from Point 5. The azimuthal angle ϕ is measured from the x-axis in the (x, y) plane while the polar angle θ is measured from the z-axis. Pseudorapidity is defined as $\eta = -ln[\tan\frac{\theta}{2}]$. The transverse momentum to the beam direction is denoted by p_T=$\sqrt{p_x^2 + p_y^2}$ and the transverse energy is denoted by E_T=$\sqrt{p_T^2 + m^2}$.

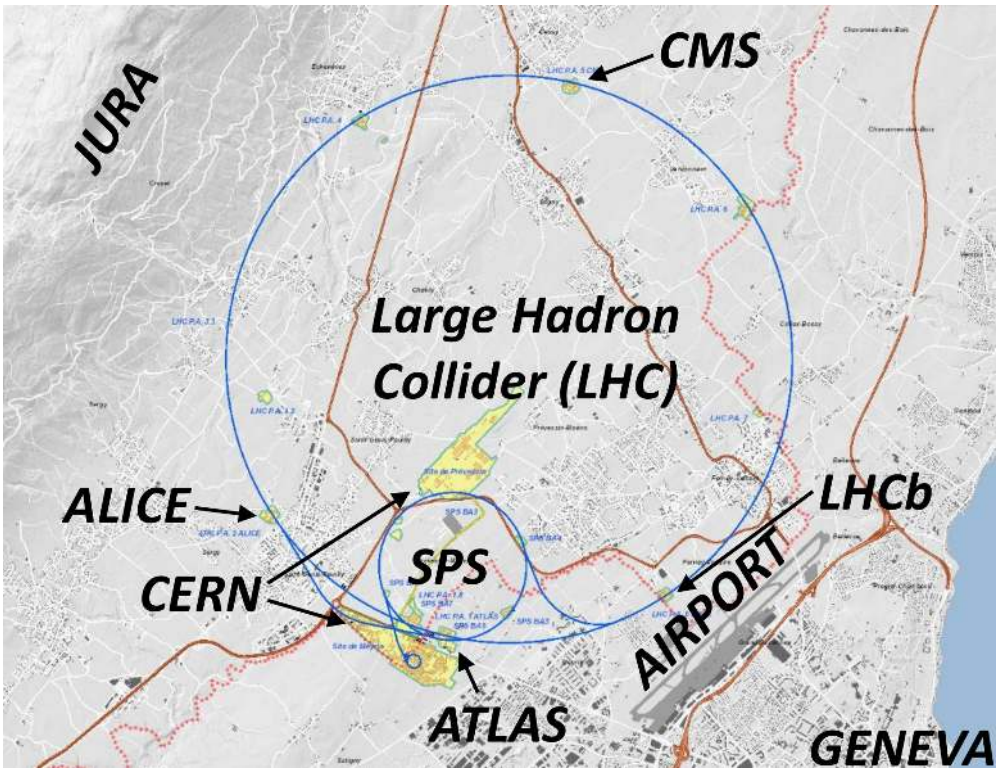


Figure 2.3: Location of CERN, accelerators and experiments.

2.1 Superconducting solenoid

The CMS detector, as its name suggests, is a compact "onion like" structure of subdetectors including a magnetic solenoid. In order to precisely measure the momentum of the high-energy particles, high-magnetic field is needed. CMS detector includes one large, superconducting solenoid capable of producing a magnetic fuild of 4 Tesla. It is the world's largest in size and field, superconducting solenoid magnet ever built. The solenoid diameter is large enough for the tracker and the calorimeters to be placed inside it. The iron yoke is outside of the solenoid, thus the magnetic field is almost completely closed. The CMS solenoid can be grouped into three main headings [12]:

- *The yoke, consisting of the barrel, the vacuum tank and the two endcaps.* The barrel yoke is splited into five barrel rings, having each a mass of 1,200 tonnes, that can move in the axial direction on heavy duty air-pads to give access to the barrel muon stations. Each endcap yoke, is built from three independent disks that can be moved on carts, supported by heavy-duty air pads, and separated to provide access to the forward muon stations and inner sub-detectors.

- *The superconducting coil, is producing 4T magnetic field.* The coil is 12.5 meters long and has an inner diameter 5.9 meters. To produce the 4T magnetic field, the 20.000 Ampere current flows through the coil.

- *The ancillaries, consisting of the external cryogenics, the power converter and circuit, and the control system.* The coil is cooled by helium circulating at temperature 4.4° K in the thermosiphon mode.

2.2 Silicon tracker

The inner tracking system of CMS is designed to provide a precise and efficient measurement of the trajectories of charged particles emerging from the LHC collisions. Charged particles flying through the tracker experience the Lorentz force by the magnetic field and they follow a spiral trajectory. The Tracker determines the charged particle track close to the interaction point, that is crucial for accurate track reconstruction, momentum measurement and particle type identification.

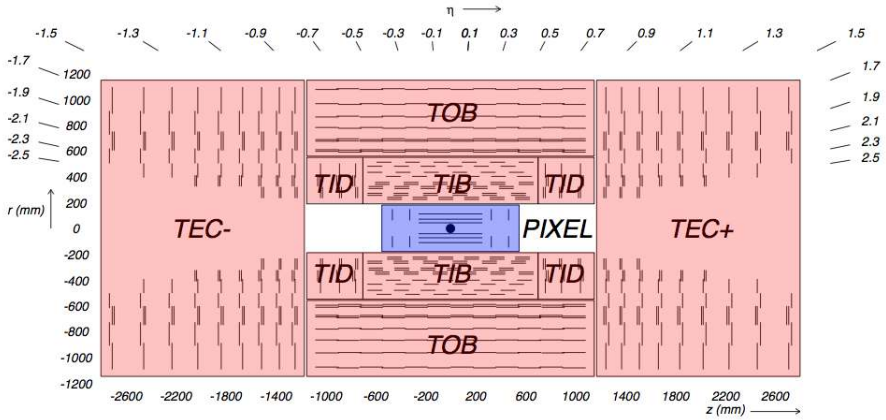


Figure 2.4: The CMS tracker

The charged particles passing through silicon generate the electric signals, which are then amplified, readout and analysed by dedicated electronics. The silicon tracking system is composed of two parts. The pixel detector is placed in the innermost region and the silicon microstrip detector in the outer region [13]. The pixel detector consists of three layers and its longitudinal cross-section is showed in Figure 2.4 with purple color. The silicon microstrip sensors consist of ten layers in the barrel, and twelve layers in either endcap region and appears in the same Figure with pink color.

2.2.1 Pixel detector

The pixel detector has been designed to provide high granularity and radiation hardness, and it is composed of 1,440 silicon pixel sensors, in total 66 million pixels, covering an area of 1000 mm by 380 mm (z, r). The CMS pixel detector can be divided into a Barrel region (BPIX) and a Forward region (FPIX). Those two regions of the detector are mechanically and electrically separated. The BPIX is composed of three identical cylindrical layers placed around the beam pipe. The FPIX is made up of two endcap disks, placed at both side of the BPIX transversally to the beam axis at ± 34.5 and ± 46.5 cm from the nominal interaction point. The placement of the two regions provides a three-hit coverage for all tracks in a pseudorapidity range up to $|\eta| = 2.5$. The three hits allow a good estimation of the track parameters, thus the information from the pixel detector is used in the on-line event selection.

The pixel detector is going to be upgraded during the long shutdown 2. The upgraded detector will contain four layers in the barrel and three disks in the endcap region instead of three and two respectively [14, 15].

2.2.2 Strip detector

The Silicon Strip Tracker covers an area of 206 m^2. The sensors are arranged in a total number of about 15,000 modules, which consist of one or two strip sensors together with the associated readout electronics.

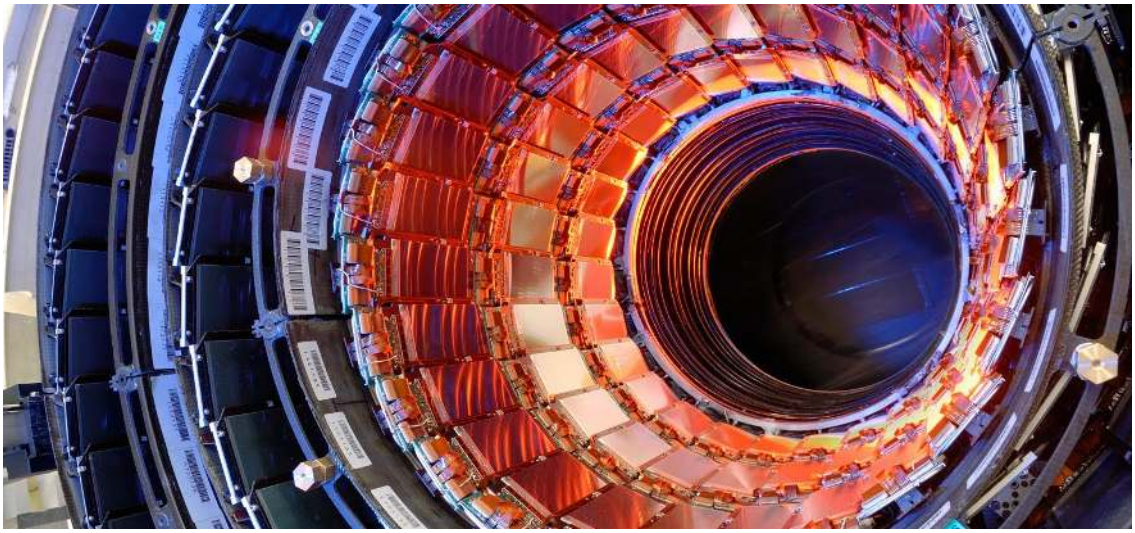


Figure 2.5: The inner endcap (TID) of the strip detector

There are several kind of strip sensors depending on the position within CMS. They are grouped in two geometrical categories, the barrel and the endcap. The silicon strip detector (tracker) consists of four inner barrel (TIB) layers assembled in shells with two inner endcaps (TID), each composed of three small discs. The outer barrel (TOB) consists of six concentric layers. Finally, two endcaps (TEC) close off the tracker [16].

2.3 Electromagnetic Calorimeter

The CMS Electromagnetic Calorimeter (ECAL) surrounds externally the tracker and is designed to measure the energy of electrons, positrons and photons. ECAL covers a pseudorapidity up to $|\eta| < 2.5$ and is composed of 75,848 lead-tungsten ($PbWO_4$) crystals [17].

The lead-tungstate crystals have a very good stopping power because of the high density (8.28 g/cm^3), their small Moliere radius (2.19 cm) and the low radiation length $X_0 = 0.89$ cm. It is worth mentioning that the crystals are transparent despite the fact that they consist 98% of lead. Those characteristics make the ECAL a small and dense detector suitable to absorb the energy of electrons and photons while passing through it. Their electromagnetic showers result in cascades giving rise to scintillations in the crystals. The signals are collected by two different types of photodetectors. The crystals in the Barrel area (ECAL Barrel, EB) are read with the help of Avalanche Photo Diodes (APD) while Vacuum Photo Triodes (VPT) are used in the Endcap area (ECAL Endcap, EE) as they are more radiation resistant.

The ECAL shown in the Figure 2.6 is divided in three main parts:

- *The EB* consists of 36 supermodules while each supermodule has 68 trigger towers and each trigger tower has 5x5 array of lead-tungstate crystals. The EB is capable to measure energy at a pseudorapidity of $|\eta|$ <1.48. The crystals have a front face area of 2.2 cm by 2.2 cm, a length of 23 cm.

- *The EE* consists of 4 Divided half EE (DEE) and each DEE consists of 3,662 tapered crystals with a frontal area of 2.68 x 2.68 cm^2 and a length of 22 cm. The crystals in each DEE are organized into 138 standard 5 x 5 supercrystal units, and 18 special shaped supercrystals that are located at the inner and outer radius. The EE covers a pseudorapidity of 1.48< $|\eta|$ <3.

- *The preshower detector* consists of two lead/silicon detector layers and is placed in front of the EE (1.653< $|\eta|$ <2.6). Its primary function is to detect photons with good spatial resolution in order to perform π^0 rejection. It is made of two disks of lead absorber, and of two planes of silicon strip detectors.

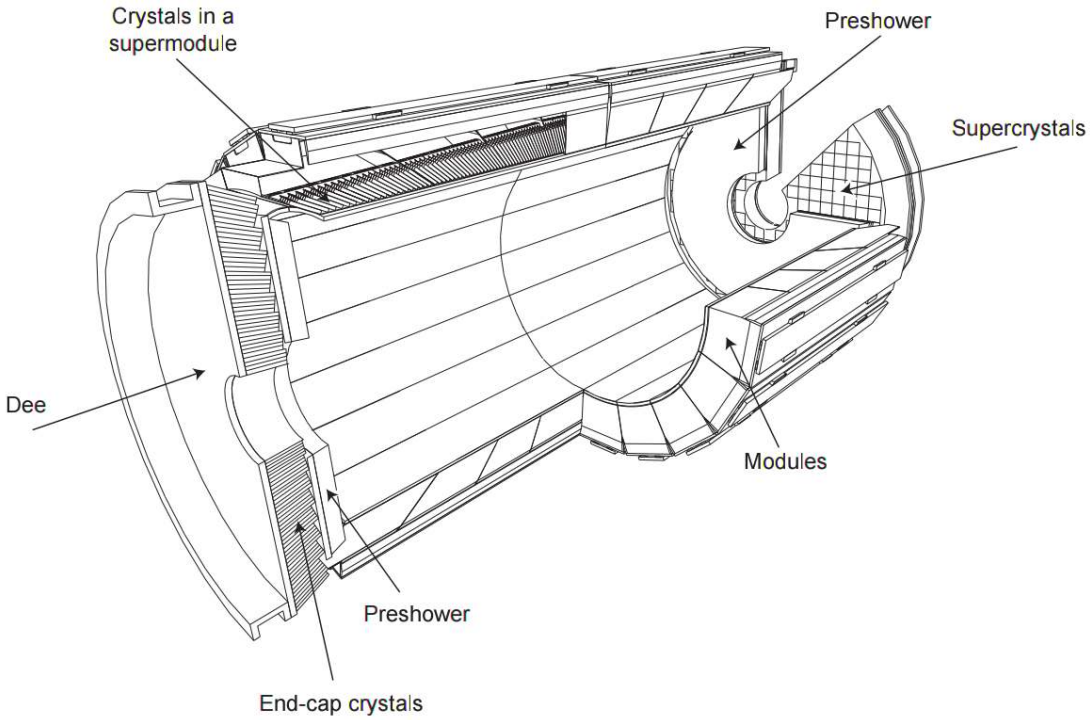


Figure 2.6: The layout of ECAL

2.4 Hadron Calorimeter

The Hadron Calorimeter (HCAL) measures the energy of hadrons and hadronic jets. To measure the energy of hadrons, the HCAL detectors cover the large $|\eta|$ <5 region. To achieve that HCAL is divided to three different detectors, shown with blue color in Figure 2.7: the Barrel HCAL (HB), covers a pseudorapidity region $|\eta|$ <1.3, the Endcap HCAL (HE), adsorbing hadrons in reagion 1.3< $|\eta|$ <3 and the Forward calorimeter (HF), which is the farthest detector from the interaction point and covers the region, 3< $|\eta|$ <5 [18]. There is one additional hadronic calorimeter

detector called Outer Barrel Calorimeter (HO), which is situated outside the coil, in order to ensure that there are no energy leaks.

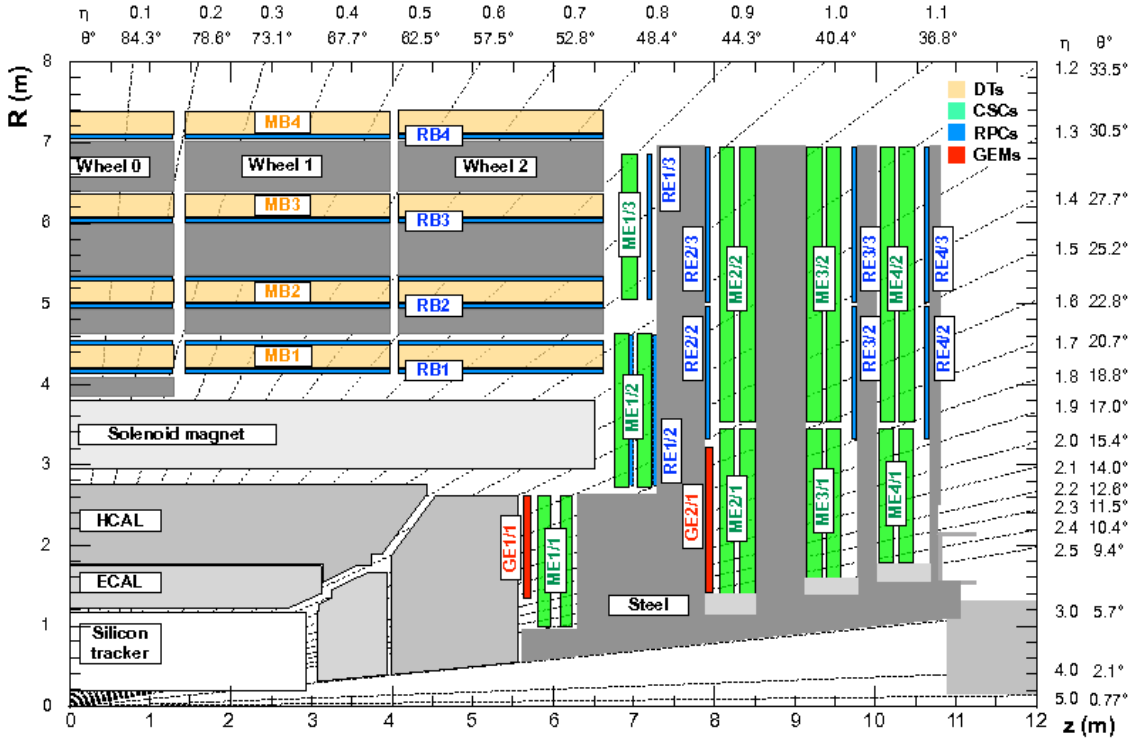


Figure 2.7: One quarter of CMS and the three HCAL detectors

There are 36 HB "wedges" divided to 2 half barrels, each weighing 26 tonnes. Similarly, 36 HE "wedges" divided to 2 half endcaps measure particle energies as they emerge through the ends of the solenoid magnet.

High-energy hadrons (protons, neutrons, pions, kaons) interact with the high-density material of the HCAL and initiate the showers of secondary particles. For the HB and HE, a sampling calorimeter composed of non-magnetic brass absorber with short interaction length and plastic fluorescent scintillator tiles was chosen. In the HF region, steel absorbers and quartz fibre scintillators are used because of their increased radiation tolerance. The scintillator tiles emit blue-violet light when a charged particle passes through them. The light is read out by the embedded wavelength-shifting (WLS) fibres. The WLS shift the primary blue-violet light into the green region of the spectrum. The WLS fibres are spliced to high-attenuation length. After that optic cables carry the green light away to the readout system located at strategic locations within the HCAL detectors. Then the optical signal is converted into fast electronic signals by photosensors called Hybrid Photodiodes (HPDs). Finally the electrical signal is sent to the data acquisition system for event triggering and event reconstruction [19].

2.5 Muon System

As the name of the experiment indicates (Compact Muon Solenoid), the muon system plays a critical role in Higgs, SUSY and others studies. The muon system finds the best four muons particles and records their physical parameters. For example one important Higgs channel is consistent with two Z particles, each of them decays into two muons (Figure 2.8).

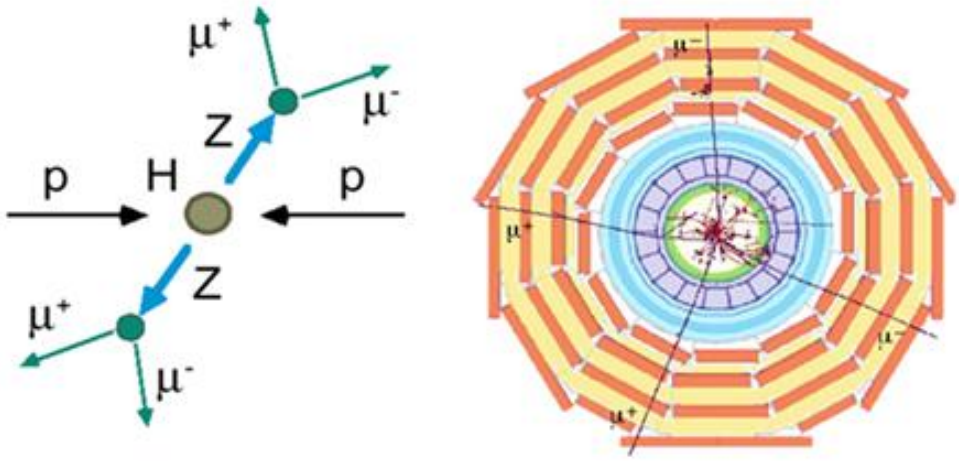


Figure 2.8: Higgs boson decay in the muon system of CMS

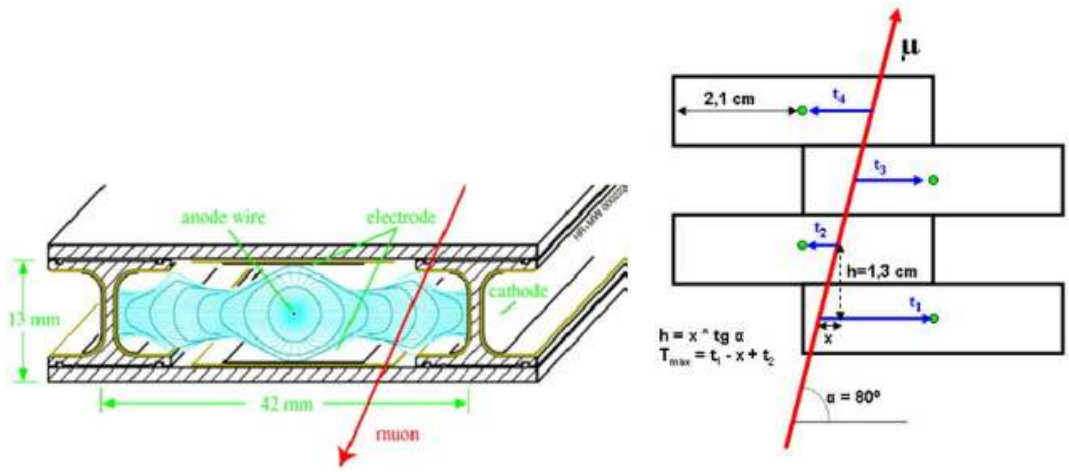
Muons in CMS are the only detectable particles that escape the inner detector layers (tracer, HCAL, ECAL) and weakly interact with matter. Being charged particles, muons bend from the magnetic field according to their velocity following a spiral trajectory. Also, muons passing through chamber detectors leave their stabs by ionizing the chamber gas. Those principles have been used to design CMS muon detectors. The muon system is divided to three types: The Drift Tubes (DTs), which exist in the muon barrel of CMS, the Cathode Strip Chambers (CSC) located in the endcaps and the Resistive Plate Chambers (RPC) spread out in both barrel and endcaps [20].

2.5.1 Drift Tubes

The DT detectors cover the barrel area of CMS with peudorapidity $|\eta|$ <1.2. DT chambers are based on 172,200 DT cells (Figure 2.9a) filled with a gas mixture of 85% Ar and 15% CO_2. In each cell there is an anode wire with high voltage. When a muon passes through the cell it ionises the gas and creates an electric charge avalanche which is collected by the wire. The maximum drift time is 380 ns and the drift velocity is about 55 mm/ns. Knowing the drift velocity and measuring the drift time, the exact position of the muon is calculated.

The cells are grouped in such a way that every time a muon passes, it ionises up to four of them (Figure 2.9b). From the drift times, the front-end electronics calculate the four positions and extract the angle a [21].

The drift tube detector is a "sandwich" of DT cells grouped in superlayers. As shown in Figure 2.10, the drift tube cells are organized in layers of ϕ and η chambers.



(a) DT cell (b) Four DT cells

Figure 2.9: Drift Tubes cell ionised by a muon

The ϕ layers (colored with blue) curries ϕ information and the η layers (colored with yellow) η information. Four layers of DT chambers make a superlayer. The DT has two ϕ superlayers and one η superlayer. As shown in the Figure 2.10 when a muon passes through the detector it ionizes the corresponding cells. Those ionized "stabs" are used from the front-end electronics to extract the ϕ and η positions and the quality (Q) of the measurement (which indicates the number of the cells ionized by the muon canditate).

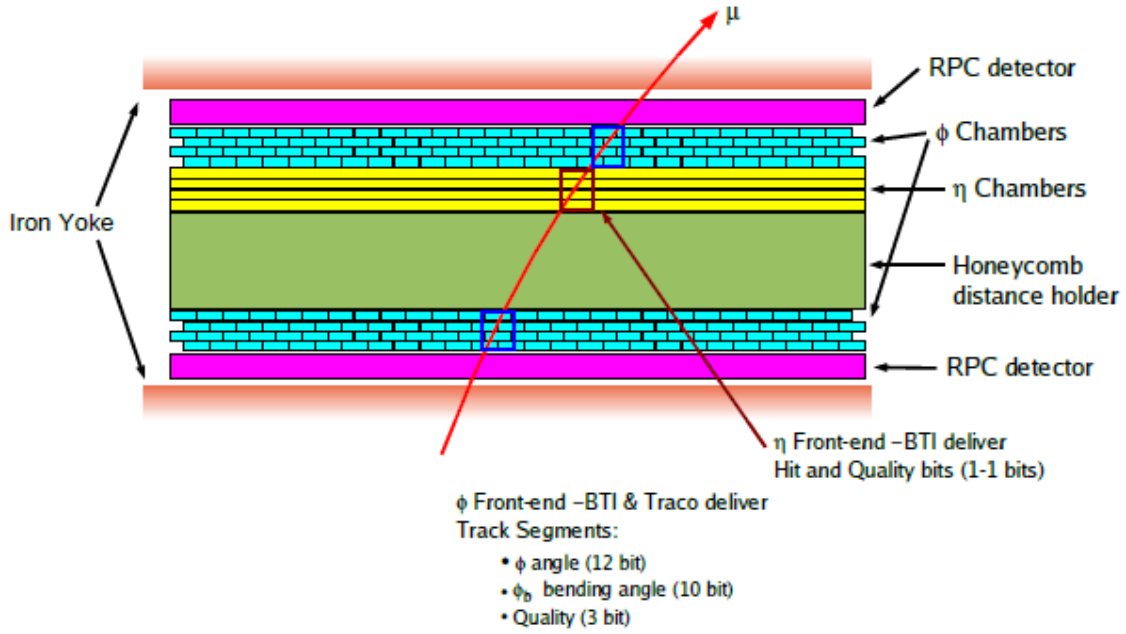


Figure 2.10: DT layers and superlayers in a DT detector

2.5.1.1 Drift Tube Minicrates

The Drift Tube MiniCrates (MCs) are attached to the DT detectors and hosts the readout and the local trigger electronics of the DTs. As shown in Figure 2.11, the MCs consist of a layer of trigger boards (TRB) and a server board (SB). The TRBs are mounted on top of the Readout boards ROBs to share chamber signals for selecting best muon candidates. Also the SB collects data from all the TRBs in a chamber and performs further track selection according to its track's quality [22]. Quality track is a rank of correlated or uncorrelated tracks between inner and outer superlayer and quality triggers (Table 2.1).

Description	Symbol	Code
HTRG on inner and outer superlayer	HH	6
HTRG on inner or outer superlayer and LTRG on inner or outer superlayer	HL	5
LTRG on inner and outer superlayer	LL	4
HTRG on outer superlayer	H_o	3
HTRG on inner superlayer	H_i	2
LTRG on outer superlayer	L_o	1
LTRG on inner superlayer	L_i	0
Null track		7

Table 2.1: Codes for track quality identifier. HTRG: High-Quality Trigger. LTRG: Low-Quality Trigger.

The main part of the TRB board is the Bunch and Track Identifier (BTI) chip. Initially, the BTI prototype was designed in FPGA but finally, it was developed in ASIC. This device does a rough track reconstruction within a superlayer and also it assigns the corresponding bunch crossing of the muon candidate. The BTI produces the local trigger in the trigger chain and generates row data.

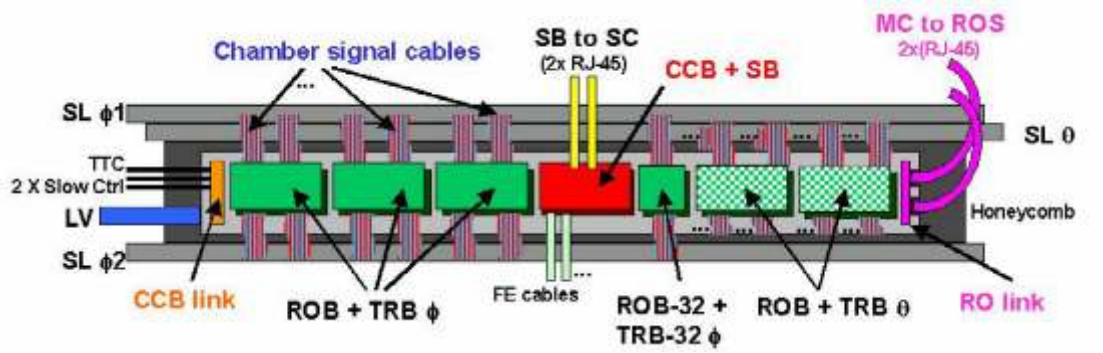


Figure 2.11: DT Minicrate

The minicrate is equipped with a data serializer that converts the output to a serial data stream and sent it over Ethernet cables in 480 Mb/s rate.

2.5.2 Resistive Plate Chambers

The Resistive Plate Chamber (RPC) consists of two parallel plates in negative voltage and between them there are parallel strips of high-positive voltage which perform the readout. The RPCs operate as any other gaseous detectors. The passing charged particle ionizes the gas. Then an electron cascade is amplified by the high voltage applied in the chamber. The anode collects the charge and finally the signal goes to the RPC readout.

The RPCs are shown in green color in the Figure 2.12. They are located in the barrel area close to the DTs and in the endcaps close to the CSCs. They cover a pseudorapidity range of $|\eta| \leq 1.6$.

As presented in the Figure 2.10, in the case of MB1 and MB2 stations, the DT is sandwiched between two RPCs. But in the other stations (MB3 and MB4), each DT has the RPCs only in the inner side. In the endcaps, the RPCs are arranged in four disks named ME1, ME2, ME3, ME4.

The RPCs have high efficiency, low noise and good time resolution (lower than 1 Bunch Crossing, 1 BX). The later is used by the trigger systems to determined the corresponding BX of the muon because the other muon detectors (DTs and CSCs) have lower time resolution.

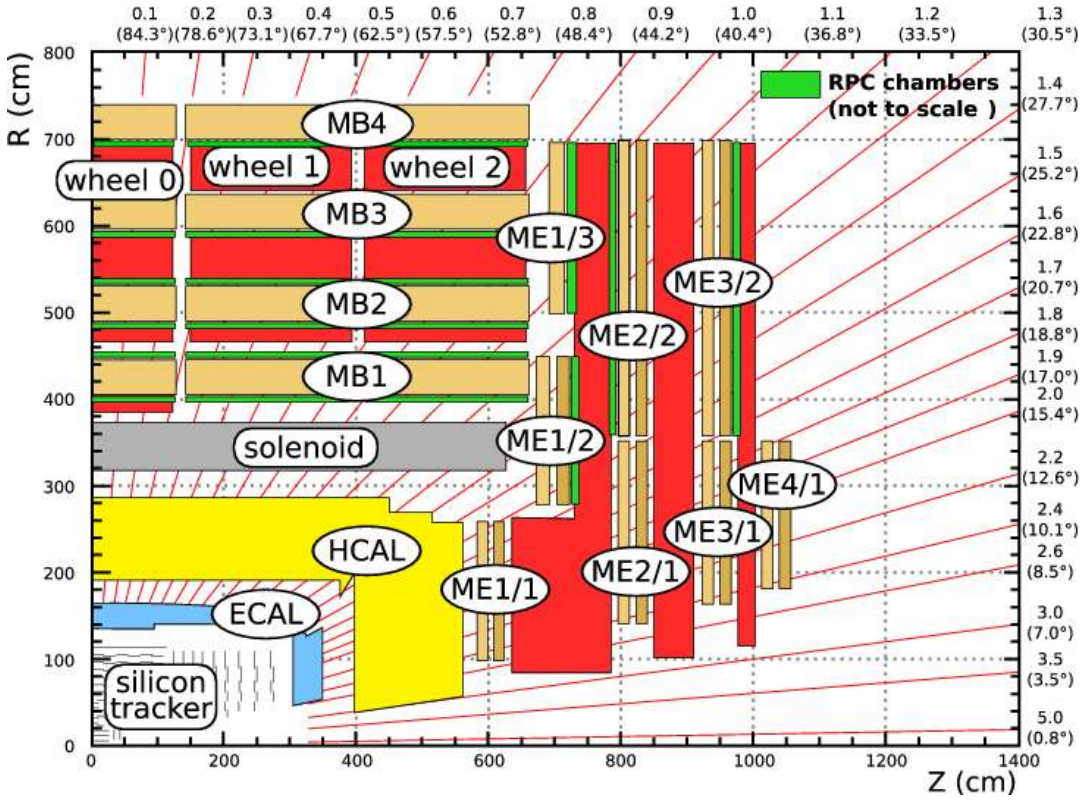


Figure 2.12: Schematic view of one quarter of CMS, in the z-ϕ plane.
RPC chambers appear with green color

2.5.3 Cathode Strip Chambers

The magnetic field of the endcaps is uneven and therefor Cathode Strip Chambers (CSCs) are used.

The CSC is a multiwire gas chamber that consists of arrays of six positively-charge wires crossed by seven negatively-charged copper strips. When a muon passes through the chamber, ionize the gas and the charge is collected by the strips and the wires. The anode wires are used for measuring the muon η coordinate, while strips provide the azimuthal angle ϕ.

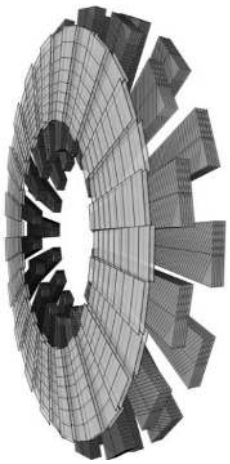


Figure 2.13: CSC ring

The Endcap muon system includes 468 CSCs. The entire system covers the pseudorapidity range $0.9< |\eta| <2.4$ and azimuthal angle 0-360^o ϕ. Figure 2.14 shows the z-ϕ plane of CMS where the CSC chambers appear in red color. The CSC chambers are organized in sectors which are grouped as ME1, ME2, ME3 and ME4. The fist group ME1, has three rings of sectors (ME1/1, ME1/2, ME1/3), each cover 10^o in ϕ. The groups ME2, ME3 consist two rings of stations (MEn/1, MEn/2, n=2, 3). The MEn/1 covers 20^o and MEn/2 10^o. Each chamber of ME4/1 covers 20^o in ϕ. The chambers have trapezoidal shape and they overlap in order to elimitate the gaps bewteen them (Figure 2.13) [23].

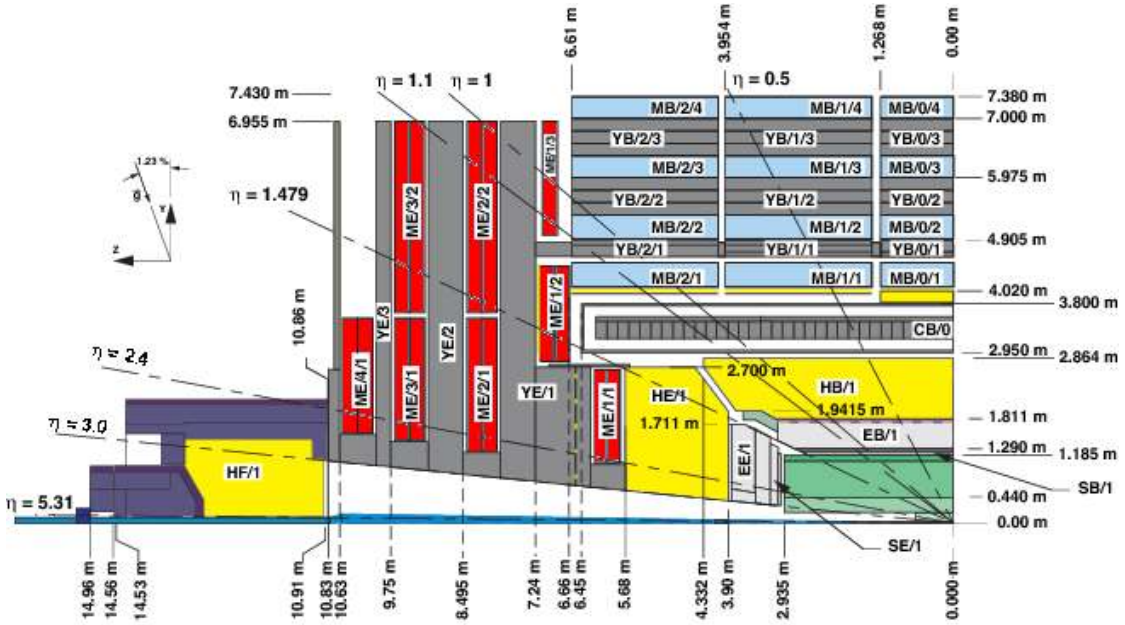


Figure 2.14: Schematic view of one quarter of CMS, in the z-ϕ plane. CSC chambers appear with red color.

2.5.4 Barrel muon apparatus

The barrel of CMS is divided to five wheels. One of them is presented in Figure 2.15. The DT detectors are shown with light blue color and the RPC with grey. They are organized in 12 sectors. Each of the sectors has four layers of DTs and three layers of RPCs. The DT are marked as *MB/Z/K/J* where Z is the number of the wheel (-2, -1, 0, +1, +2 are parallel to the Z axis of CMS), K is the number of the DT layer (1, 2, 3, 4) and J is the number of the DT sector (1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12). Equivalent, the RPC detectors are marked as *YB/Z/K/J* where Z is the number of the wheel (-2, -1, 0, +1, +2), K is the number of the RPC layer (1, 2, 3) and J is the number of the DT sector (1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12). Each DT sector covers a ϕ angle of 60^o [24]. As the Figure shows in the top and bottom sectors, the fourth layers have two DT detectors. Considering that CMS has five wheels and each wheel has 12 sectors, 60 sectors exists in total. Also considering the total number of sectors and the fact that bottom and top sectors have one more DT, 70 DTs are used. In addition to the Y-X plate (wheel), sectors are also organized to ϕ=30^o, across Z-axis were one wedge has 5 sectors (one of each wheel). As will be presented in detail in the next chapter, the barrel muon system searches muons in a wedge level.

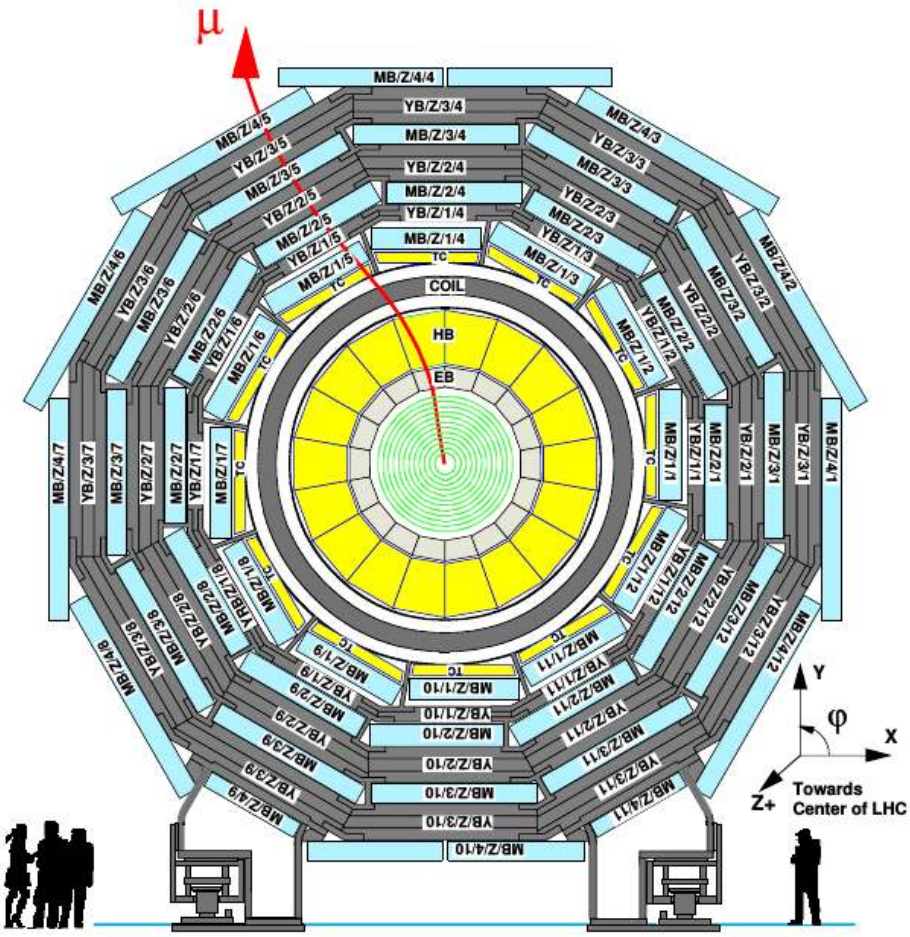


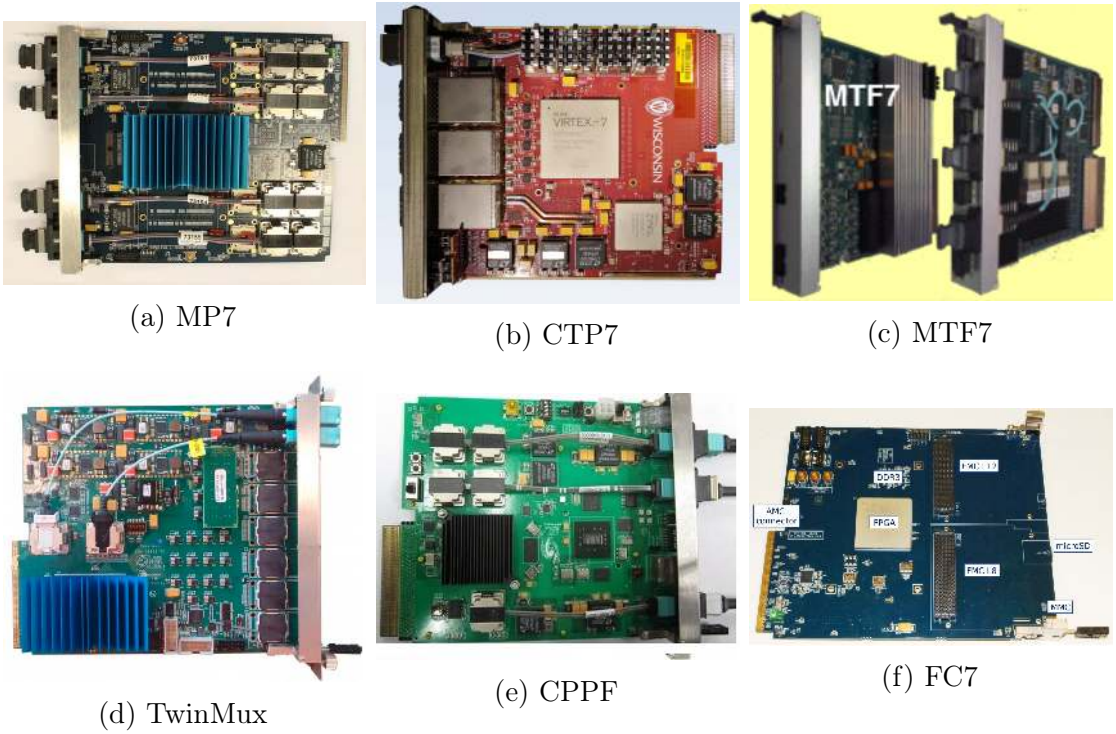
Figure 2.15: Schematic view of one of the five wheels of the barrel of the CMS experiment, in the x-y plane and a track of a muon.

2.6 Back-End electronics in CMS

New electronic systems offer stability, redundancy, high-speed protocols and high-end possessing power. Those characteristics are widely used in High-Energy Physics (HEP) experiments in the off-detector electronics (Back-End, BE) categorized as Data AcQisition (DAQ), Trigger and Control systems. CERN groups have developed electronic systems (Frond-End, Back-End, etc), based on the state of art technology, in order to design new HEP experiments and upgrade the current ones. The Front-End systems are mounted in a strategic places close to the particle detectors and eventually digitize, record and send the results over copper or optical links.

In addition, modern electronics are used in back-end systems in order to trigger on useful information and collect the detector data using DAQ systems. The back-end systems, are modular systems characterized by specification standards like the Nuclear Instrumentation Module (NIM), the widely used Versa Module Europa (VME) and the two most recent standards: Advanced and Micro Telecommunications Computing Architecture (ATCA and μTCA) [25]. Micro Telecommunications Computing Architectures is an open standard for building high-switched fabric computer systems in a small form factor. In HEP applications, Advanced Mezzanine Cards (AMC) mounted on a μTCA core, provide processing and I/O functions which are used in order to receive data from the detectors and find particles.

During the phase I trigger upgrade of CMS, which is completed in the first quarter of 2016, the old fashioned VME standard has been replaced by the μTCA [1]. Figure 2.16 shows the AMCs designed for this upgrade. The cards are installed in CMS underground cavern USC55.



(a) MP7 (b) CTP7 (c) MTF7

(d) TwinMux (e) CPPF (f) FC7

Figure 2.16: AMCs used in CMS for the phase I trigger upgrade

The AMC cards showing in Figure 2.16, use the most advanced and modern

digital devices such as switching regulators, PLLs, digital switches, microcontrollers, Complex Programmable Logic Devices (CPLDs), FPGAs, optical modules and several memories.

The most powerful digital device in applications such as trigger and readout systems of the experiments at the LHC, is the FPGA. The implemented logic on a FPGA is by nature parallel and is described mostly by VHDL or Verilog programming languages. After the compilation the results of the design can be described as many concurrent interconnections of electronic components, called netlist.

The FPGA hardware is an array of hardware components in the chip like: Look Up Table (LUT), Block RAM (BRAM), Digital Signal Processor (DSP), First-in First-out memory (FIFO), Clock Management Tile (CMT), Buffer (BUF), SERializers/DESerializers (SERDES), Transceiver, etc [26].

For example in trigger systems, algorithms are implemented using LUTs in case of simple functions and DSPs from more advanced tasks. To extract predefined values with low latency (one clock cycle) BRAM elements are used. In addition transceivers and SERDES are used in order to establish serial interfaces over high-speed optical links, medium copper connections over LVDS and ethernet connections.

Chapter 3

The CMS Trigger

As presented in the previous chapter, CMS is a complex system of detectors that finds different kinds of particles on full ϕ and η coordinates. In each detector, front-end electronics are mounted to collect analog electric signals from particle passage, convert it to digital bits and send it over serial links for consequent analysis. CMS has a large number of readout channels (100 million) which provide an average of 1 MB of data per event. Considering that the bunch crossing rate is 40 MHz, the total data stream is about 40 TB/s, which is practically impossible to store and process.

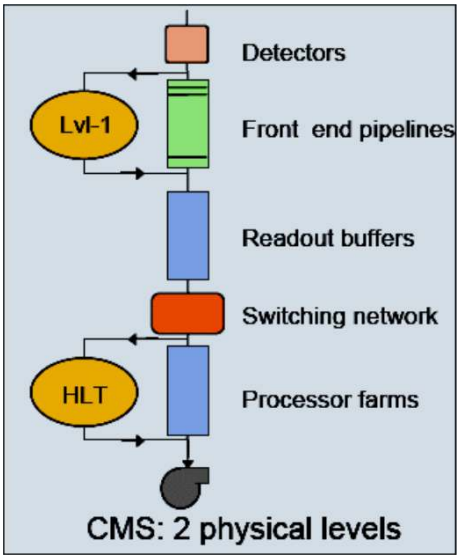


Figure 3.1: The TriDAS project

The first level (Tier 0) of the Worldwide LHC Computing Grid is foreseen to give to CMS 100 MB/s throughput. Considering the event size (1 MB), results to that only the 100 most interesting collisions out of the 40 million generating every second must be selected. This is performed by the Trigger and Data Acquisition System (TriDAS) [27]. The trigger flow diagram in CMS is presented in Figure 3.1. It is divided in two levels, the first (Level-1 Trigger, Lvl-1) reduces the input rate from 40 MHz to 100 KHz and the second level (High Level Trigger, HLT) reduces it farther to 100 Hz, with the use of a processors farm. As can be seen in the data-flow diagram, the L1 Trigger operates in parallel with the front-end pipeline memories existing in the output of the detector front-end electronics. The L1 Trigger exclusively consists of electronic systems and has a latency budget given by the pipeline memory depth (green color). This time budget is 128 long times 25 ns bunch crossings (BXs) = 3.2 us. Every time that the L1 Trigger system finds a qualified event, it generates a Level 1 Accept (L1A) signal. The L1A signal enables the data writing in the readout buffers. The readout buffers are connected to the processors in the HLT farm with a large switch network. The High-Level Trigger (HLT) online event filter system does the final triggering by using more complex (that hardware uses) algorithms compared to the L1 Trigger. Finally the output of the TriDAS stream (rate 100 Hz of 1 MB event size) is forwarding for storage and data analysis to a global computer farm (GRID).

3.1 The CMS Level 1 Trigger

After the phase-I upgrade of LHC, the instantaneous luminosity as well as the average pile-up in CMS expected to be doubled. Moreover, after phase-II upgrade (2025), the luminosity will be increased farther and reach to $5x10^{34}$ $cm^{-2}s^{-1}$, and this unfortunately exceeds the initial design specifications of the L1 Trigger (L1T) and Trigger Primitive Generator (TPG[1]) in CMS. High-luminosity affects trigger performance by introducing higher-trigger rates (with potential spikes) as well as lower trigger efficiency. To compensate with the LHC machine upgrades, the Level 1 Trigger system has radically changed. The new system, installed after the phase-I upgrade, has increased its flexibility and therefore offers adaption over the rapidly evolving running conditions. Flexibility has been accomplished by using the telecommunications standard μTCA which replaced the previously used VME framework. The μTCA systems are modular, offer higher bandwidth and hot-swapping. New Advanced Mezzanine Cards (AMCs), specially designed for CMS L1 trigger upgrade are based on modern, large FPGAs and big memories in order to implement the trigger logic. The use of many high-bandwidth optical links (10 Gb/s) offers a large scale fan-out to different trigger processors and increases farther the flexibility improving the robustness [1, 28].

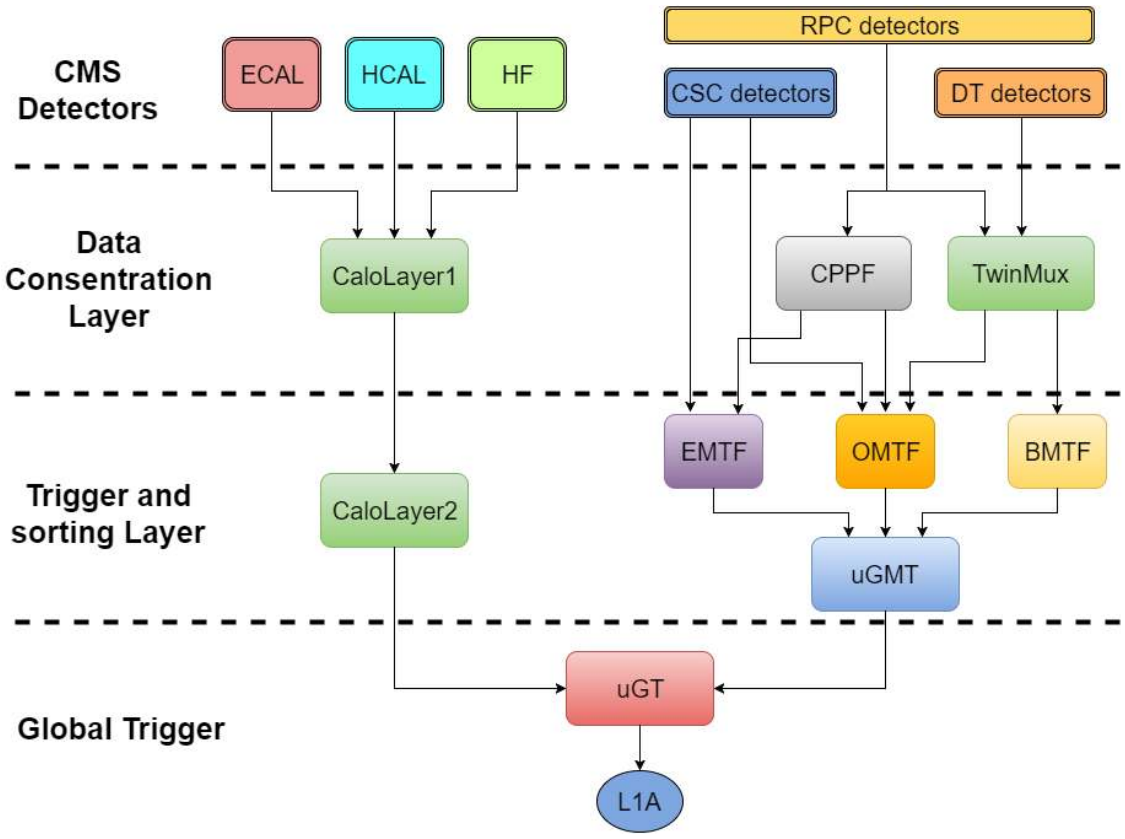


Figure 3.2: The upgraded L1 Trigger architecture and data flow of CMS

The dataflow diagram of the L1 Trigger after phase I upgrade is shown in Figure 3.2. There are two main trigger branches: the calorimeter trigger branch, shown on the left side of the trigger tree and the muon trigger branch, shown on the

[1]TPGs are object produced by the detector electronics every 25 ns.

right side. The L1 Trigger data flow can be categorized in four layers: the detector layer, the data-concentration, the regional-triggers and the global-trigger layer. The CMS detectors systems (ECAL, HCAL, HF, RPC, CSC and DT) introduce Trigger Primitives Generators (TPGs). The TPGs produce row data after a particle detection. These data, called Trigger Primitives (TPs), contain information about the local energy absorption or the particle hits, local ϕ and η position, the quality of the measurement and the bunch crossing to which the measurement should be assigned. The TPGs logic reconstructs the detected information from the continuous stream of digitizations at the LHC bunch crossing frequency. In the data concentration layer, data primitives from different TPGs are collected, synchronized with the LHC clock and forwarded to the next trigger layer called trigger and sorting layers. In data-concentration layer, short local algorithms are also performed in order to move the trigger redundancy detection as much as earlier in order to obtain a higher-trigger performance with higher efficiency and rate reduction. Track finding, energy sum and jet clustering are performed in the trigger and sorting layer. This layer includes parallel algorithms running on parallel systems (in case of muons). The regional trigger algorithms generate events located in the corresponding regions. Then the cancel-out algorithm cuts duplicate events and sort the results according to specific conditions. The final level-1 trigger layer is the micro Global Trigger (μGT). It collects the results from the two branches, implements "the *menu* of triggers" (a set of selected requirements applied to the final list of objects) and generates the so-called "*finalOR*" signal which triggers the readout of the detectors and is the basis for further calculations in the High Level Trigger.

3.1.1 Calorimeter Trigger

The Calorimeter Trigger applies the Time Multiplexing Trigger (TMT). This algorithm finds energy jet, tau, and electron/photon candidates. The logic is divided into two layers that during the L1 Trigger Upgrade have replaced the Regional and the Global Calorimeter Trigger. The Figure 3.3 shows both legacy (left) and upgraded (right) calorimeter trigger with their interconnections. The L1 Trigger Calorimeter Upgrade has been proceeded in two stages. The first established in 2015 and the second in 2016. In the first stage, Layer-2 Calo Trigger replaces the Global Calorimeter Trigger (GCT) hardware and in the second stage, Layer-1 Calo Trigger replaces the Regional Calorimeter Trigger (RCT). Additionally to the two Calo processor Layers three different kinds of cards are used in order to split and transmit data though optical links. The optical Serial Link Board (oSLB) duplicates ECAL TPs from the existing ECAL back-end. The optical Receiver Mezzanine (oRM) is used in the RCT to receive data from ECAL (via oSLB) and HF. Finally, the optical Regional Summary Card (oRSC) sends the RCT data to GCT, Layer 1 Calorimeter Trigger and Layer 2 Calorimeter Trigger [29].

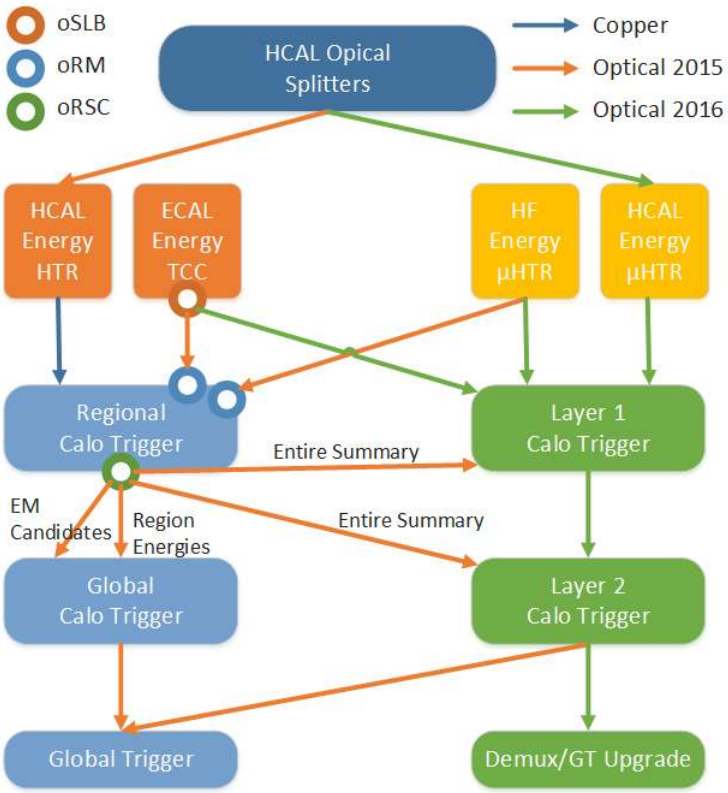


Figure 3.3: The Level-1 Calorimeter Trigger of CMS before and after the upgrade. On the left side is the old system and on the right side the upgraded system. The upgrade lasted for two years. In that period parts of the new system was getting in charge of the calorimeter trigger stage by stage.

Figure 3.4 shows the L1 Calorimeter crates and patch panel. On the left side is the CaloLayer1 and on the right side the CaloLayer2. The CaloLayer1 sends and fan-out data to the CaloLayer2 via optical spliters (Molex FlexPlane) inside the patch panel.

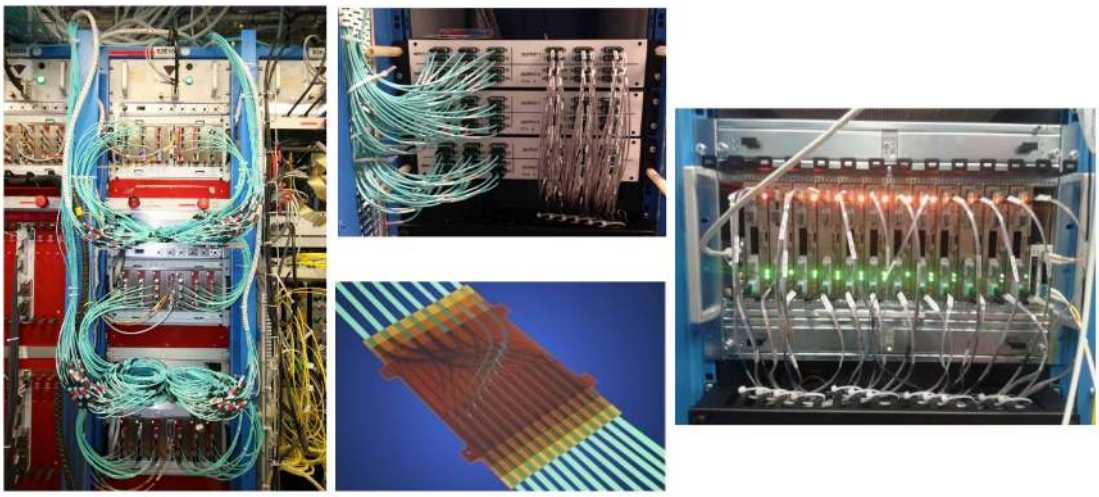


Figure 3.4: The Level-1 Trigger Calorimeter system. On the left is the CaloLayer1. On the right is the CaloLayer2. On the top middle is the patch panel. On the middle bottom is the Molex FlexPlane.

3.1.1.1 Calorimeter Layer 1

The first layer of the calorimeter Trigger (CaloL1) receives ECAL, HCAL and HF Trigger Primitives (TPs) data using synchronous 4.8 Gb/s and 6.4 Gb/s protocols. The CaloLayer1 contains logic that pre-processes all Trigger Primitives from ECAL HCAL and HF detectors for each bunch-crossing. Then it synchronizes and transmits the results to the second trigger Calorimeter Layer called, CaloL2. The Calorimeter Trigger Processor-Virtex7 (CTP7) card (Figure 3.5) has been designed by the University of Wisconsin. The processing power is based on the 690T Virtex-7 FPGA which gives the required resources in order to synchronize the inputs, apply the pre-processing algorithm and re-transmit the data to CaloL2. The card uses minipods to receive 31 channels and transmit 12 channels. Also it uses three CXP transceivers capable to transmit 36 I/O serial links running at 10 Gb/s. The CTP7 card is controlled by an embedded operating system (OS) based on the hybrid ASIC/FPGA chip (ZYNQ-045). This device hosts an FPGA with a ARM-CPU in the same die. CTP7 uses the OS to access and control the FPGA via a chip2chip interface. Also it uploads firmware to the FPGA thought scp protocol and stores it to the micro Secure Digital (μSD) memory. In addition the ZYNQ System on a Chip (SoC) controls the optics of the card and configures the reference clock generator (SI5324) that feeds the GTHs of the Virtex-7 FPGA. CTP7 also uses a 32-bit Atmel microcontroller to implement IPMI and communicate with the μTCA back-plane. Finally, it has a CPLD for switching the JTAG chain routing [30, 31].

Figure 3.5: The CTP7 processor with three CXPs used in the CaloL1.

The CaloL1 Back-End (BE) μTCA system consists of 3 μTCA crates each one having 6 CTP7s. It receives trigger primitives with 4.8 Gb/s and 6.4 Gb/s links, synchronizes them and transmits the results to the CaloL2 using an Asynchronous 10-Gb/s protocol. CaloL1 has moved the redundancy earlier in the trigger chain by calculating trigger tower sums from different TPs.

3.1.1.2 Calorimeter Layer 2

The Calorimeter Layer 2 (CaloLayer2) uses Master Processors virtex-7 (MP7s) designed by Imperial College (Figure 3.6) in order to trigger physics objects from the calorimeter detectors. The MP7 has 72-input and 72-output optical links operating at 10 Gbps. It uses 12 minipod optics with MTP-48 connectors. The large scale 690 Virtex-7 Xilinx FPGA, used in the MP7, is capable to implement the algorithm of the CaloLayer2 and the required infrastructure. The atmel AT32-UC3A-3256 mircocontroller of the card, handles the Intelligent Platform Management Interface (IPMI) between the card and the μTCA backplane. The Xilinx CPLD of the MP7 does the switching of the JTAG rooting in the card. The MP7 is powered by the LTM4606 regulators (from LINEAR technology), specific designed for transceiver applications [32]. The card is accessible by IP-UDP protocol thought the microcontroller (MMC) that initialize the connection on power up. This is achieved after the MMC gets the MAC address from the card and request an IP address from a RARP service provided by a control PC. MP7 processors are used in the CaloLayer2 as well as in the Barrel Muon Track Finder, in the Global Muon and Global Trigger systems.

Figure 3.6: The Master Processor Virtex-7 (MP7).

Calorimeter architecture: The CaloLayer2 implements the main part of the calorimeter algorithm, called Time-Multiplexed Trigger (TMT) [33, 34]. The first MP7 of the CaloLayer2 receives data of one bunch crossing from CTP7s and performs the reconstruction and identification of physics objects. A second MP7 receives data of the next bunch crossing and runs the same algorithm. This procedure is repeated until the tenth MP7 receives data from the tenth bunch crossing. The processing time of the TMT is available through the use of a pipeline. With this architecture every MP7 collects energy sums of ECAL and HCAL from all calorimeters. Output trigger data are then sent to the micro Global Trigger. The TMT algorithm is shown in Figure 3.7. From the one hand, two output links from each CTP7 are connected to each MP7 (24 output times 36 CTP7s equals to 864 links to 12 MP7s). From the other hand, 72 serial links of the MP7 are used to connect to 36 CPT7 boards from Layer-1 (72 inputs times 12 MP7s equals to 864 links from 36 CTP7s) [35].

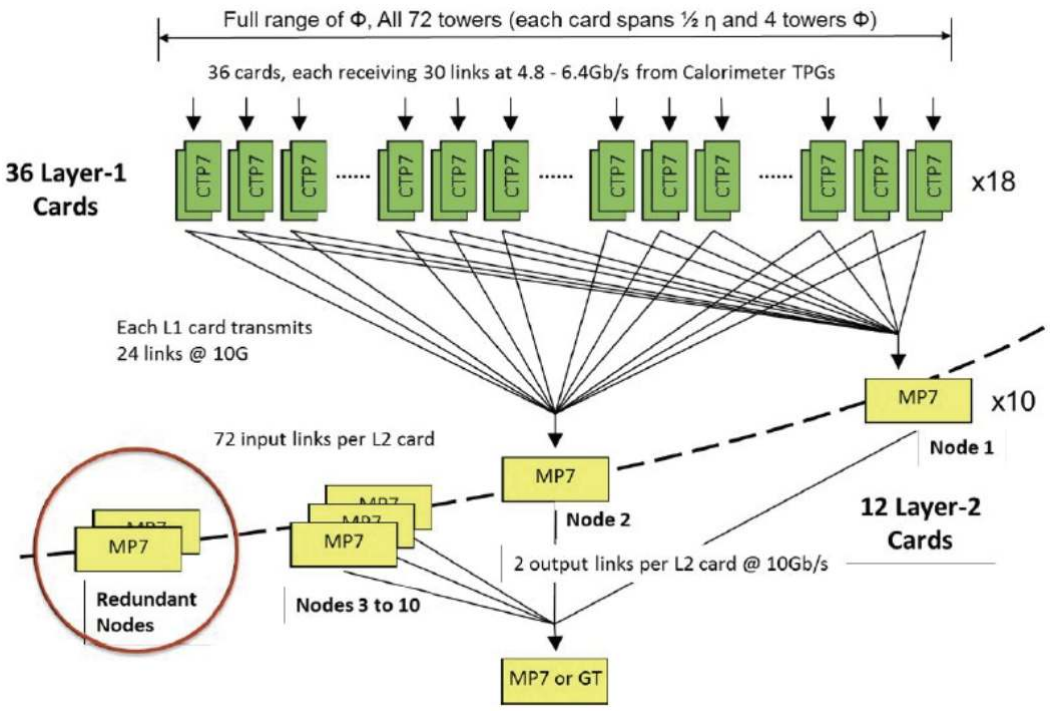


Figure 3.7: Time Multiplexer Trigger (TMT) architecture.

3.1.2 Muon Trigger

The block diagram of the L1 muon trigger of CMS is shown in Figure 3.8 and is divided in four layers. The first layer includes the Trigger Primitive Generators (TPGs) which lie on the Front-End of the detectors. In the second layer, data concentrators are responsible for pre-possessing the primitives (first step of the algorithm) and fan-out the results in the subsystems of the 3rd layer. The third layer includes the regional-trigger processors for muon-tracks determination. Finally, in the micro Global Muon Trigger (μGMT) the best eight muons from all track finders are selected. The muon L1 trigger is divided in three subsystems representing three η areas of the muon detectors in CMS. The Barrel Muon Track Finder (BMTF), the Overlap Muon Track Finder (OMTF) and the Endcap Muon Track Finder (EMTF). They are searching for muon tracks in $|\eta|$ <0.83, 0.83< $|\eta|$ <1.24 and 1.24< $|\eta|$ <2.4 respectively [1]. The RPC detectors are spread in both barrel and endcaps while DTs exist in the barrel and CSC in the endcaps region. As with the CaloLayer1 of the Calorimeter Trigger, where the data are concentrated, pre-processed and fanout, a similar operation is performed in the CPPF and TwinMux of the Muon Trigger. DT, RPC and HO TPs are received at TwinMux while the RPC TPs are receive at CPPF. The TwinMux combines DT data with RPC from the barrel and generates the so-called, super-primitives. Then it sends the result to the BMTF and OMTF track finders. The CPPF receives RPC data from the endcap region and sends them to EMTF and OMTF. Data from CSC are send directly to both EMTF and OMTF. The three track finders identify totally up to 108 muons for every bunch crossing (BX). Finally, the μGMT selects the best eight muons according to the higher rank (formed by p_T and quality) and transmit them to the Global Trigger.

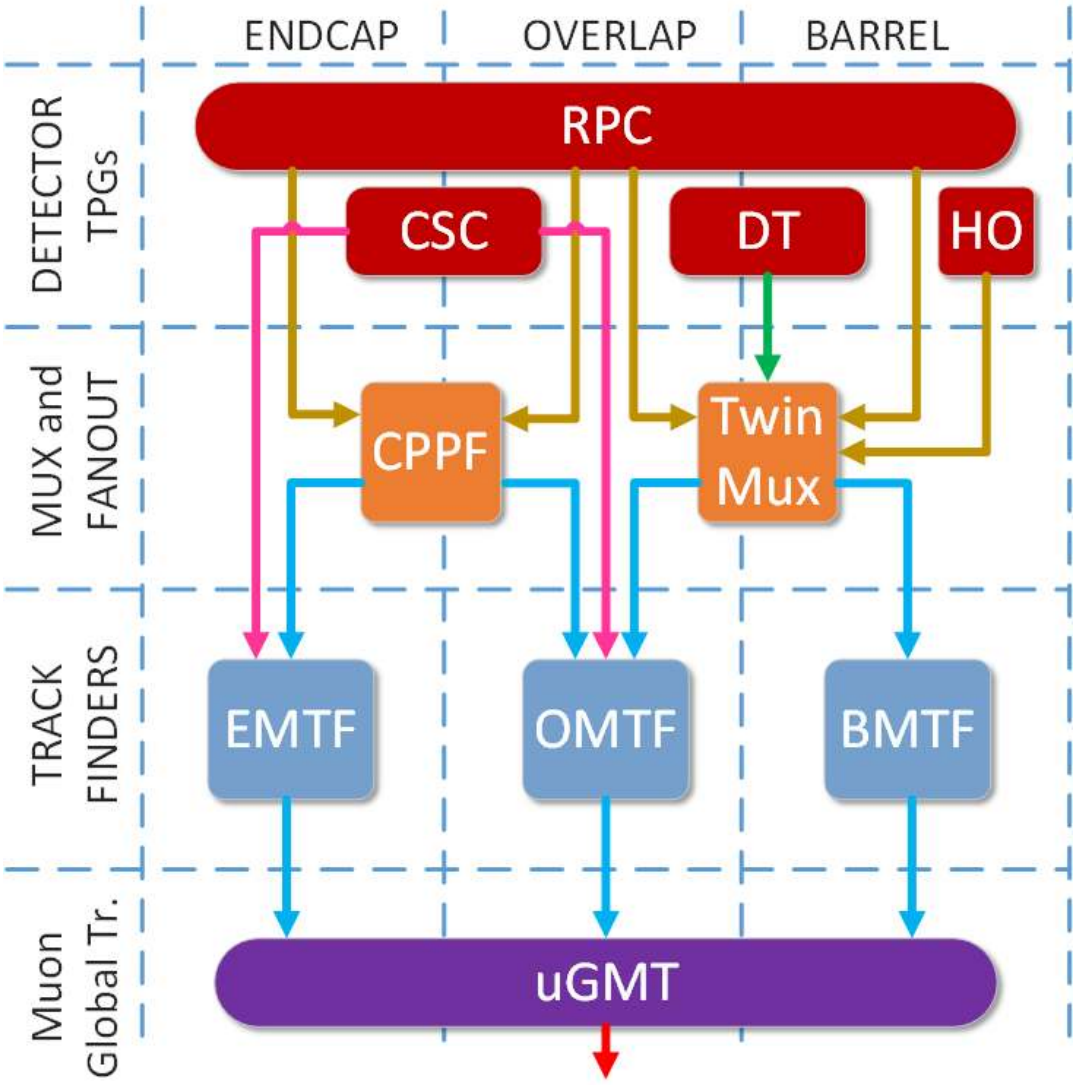


Figure 3.8: The L1 Muon Trigger architecture of CMS after the phase I upgrade. The color of the arrows indicates the transmission protocols used with optical links. Green: synchronous 480 Mb/s, Brown: synchronous 1.6 Gb/s (GOL links), Pink: synchronous 3.2 Gb/s and Blue: asynchronous with the LHC clock, 10-Gb/s links.

3.1.2.1 The upgraded sector collector - TwinMux

The TwinMux system has replaced the old Trigger Sector Collector (TSC) used in Muon Trigger of CMS until December 2015. The TwinMux as it already mentioned collects, synchronizes and distributes the Trigger Primitives (TPs) to the track finders. The same hardware will be used to replace the current Read Out Server (ROS) with the new readout, called micro Read Out Server (μROS), which will receive data from the DT minicrates after they get the L1 accept signal. The μROS is part of the Data Aqusition and not of the Trigger system [36, 3].

The TwinMux card is shown in the Figure 3.9. The card hosts a Virtex-7 FPGA, part *XC7VX330TFFG1761-3* and an ATmega128 microcontroller. Also it has minipod and SNAP12 optics [37], a CPLD to control the JTAG routing and switching regulators to provide the power on the card. The ATmega128 plays the role of a Module Management Controller (MMC) whose main operation is the power

management of the card. The FPGA is connected to the SNAP12 optics through its SERDES or through its GTH transicevers. The selection of the routing is done by placing a small mezzanine card on the board. The TwinMux uses the SNAP12s to receive data from the DT minicrates with optical links of 480 Mb/s bandwidth and from RPC minicrates using 1.6-Gb/s links. The FPGA transmits the results to the next stage using 10-Gb/s links through minipods.

Figure 3.9: The TwinMux card. This AMC card uses a Virtex-7 FPGA that pre-processes TPs and transmits them to the track finders using optical links.

Each TwinMux collects all TPs from one muon sector of the barrel. The Figure 3.10 shows the input and output links of one TwinMux. It receives TPs of DT using 32 synchronous links at 480 Mb/s (green color), 3 synchronous links at 1.6 Gb/s links (brown color) and transmit 12 asynchronous links at 10 Gb/s (blue color).

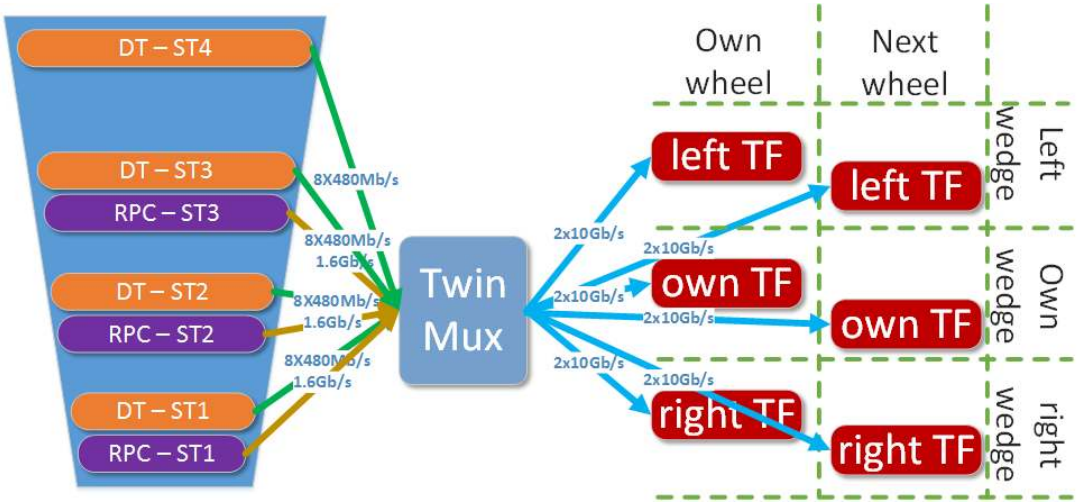


Figure 3.10: Block diagram of the TwinMux serial I/Os.

As is shown in Figure 3.10, each TwinMux card multiplicates (fan-out) its output to six Track Finders (TFs) and delivers the same TPs using 2 x 10 Gb/s links for every TF. This fan-out gives to neighbor TFs all the information in order to search for muons that cross a DT chamber of the same sector (co-called "own sector") and continue the trajectory passing through DT chambers of neighbor sectors.

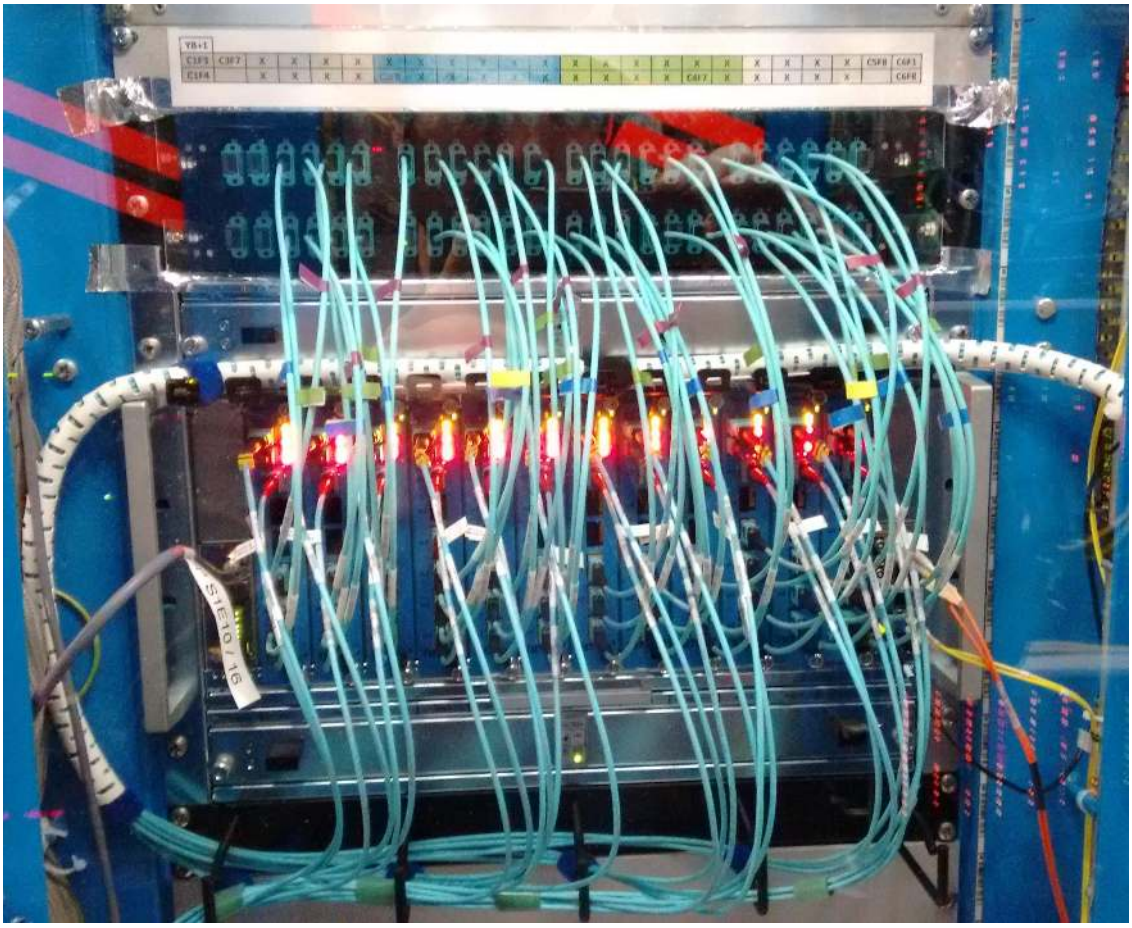


Figure 3.11: TwinMux crate.

60 (12 sectors times 5 wheels) TwinMuxs are used to cover all DT sectors and they are hosted in five μTCA crates according to their relative DT wheel. Therefore 12 TwinMuxs are placed in each crate one out of the five crates installed in the CMS USC55 cavern. The Figure 3.11 shows one TwinMux crate during operation. RPC detector provides better timing accuracy than the DT and therefore in the TwinMux algorithm the DT data are synchronized according to the RPC. This procedure increased the efficiency later in the trigger chain (BMTF). Also it is foreseen to use LUTs to convert RPC data to DT data in order to replace any potentially missing DT data (missing stabs) with RPC data.

3.1.2.2 Concentration Pre-Processing and Fan-out

The second system used to concentrate muon primitives is called Concentration Pre-Processing and Fan-out (CPPF). It receives RPC data at 1.6 Gb/s from endcaps, synchronizes and transmits them to the OMTF and EMTF.

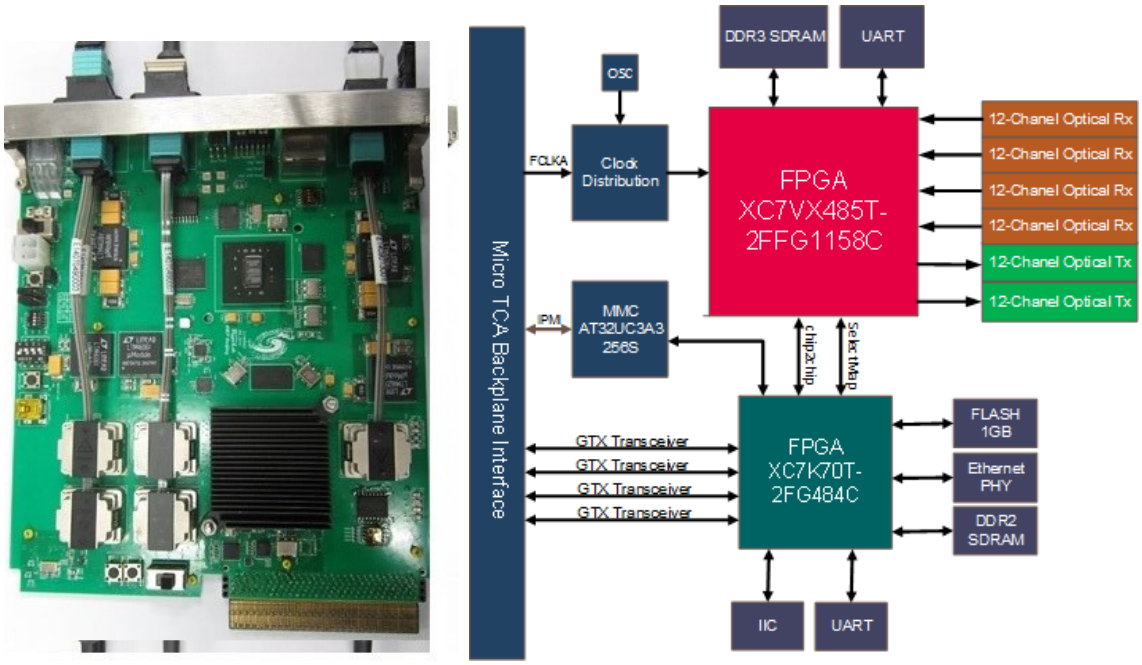


Figure 3.12: The hardware of the Concentration Pre-Processing and Fan-out card. Left: CPPF card. Right: CPPF block diagram

The hardware of the CPPF is shown in the Figure 3.12. The card has minipod optics, two FPGAs, one 32 bit microcontroller, DDR3 memory, Flash memory, I^2C and UART components [38]. The block diagram shows the interconnections of the card. This design is based in two FPGAs. One of the FPGAs, a Kintex-7 *XC7K70TFBG484-2*, called Control FPGA is used to interconnect the AMC to the network and controls several components in the card. The second FPGA, a Virtex-7 *XC7VX415TFFG1158-2*, called Core FPGA implements the main functions of the CPPF system (input links, synchronization and output links).

3.1.2.3 Barrel Muon Track Finder (BMTF)

The hardware of the track finder of the barrel muon system is shown in the Figure 3.13. It includes two μTCA crates. Each of them hosts 6 track finder Master Processors Virtex-7 (MP7). Every MP7 is searching for muons in one wedge of the muon barrel. The crates organize the MP7 in two half barrel wedges. The processors of the wedges 1, 2, 3, 4, 5 and 6 are placed in the top crate and the processors of the wedges 7, 8, 9, 10, 11 and 12 searching for muons in the bottom crate. The BMTF crate, consists of one commercial MicroTCA Carrier Hub (MCH) to access the AMCs and one AMC13 designed and constructed at CMS to connect the system with Time Control Distribution System (TCDS) and send the triggered data to Front End Driver (FED).

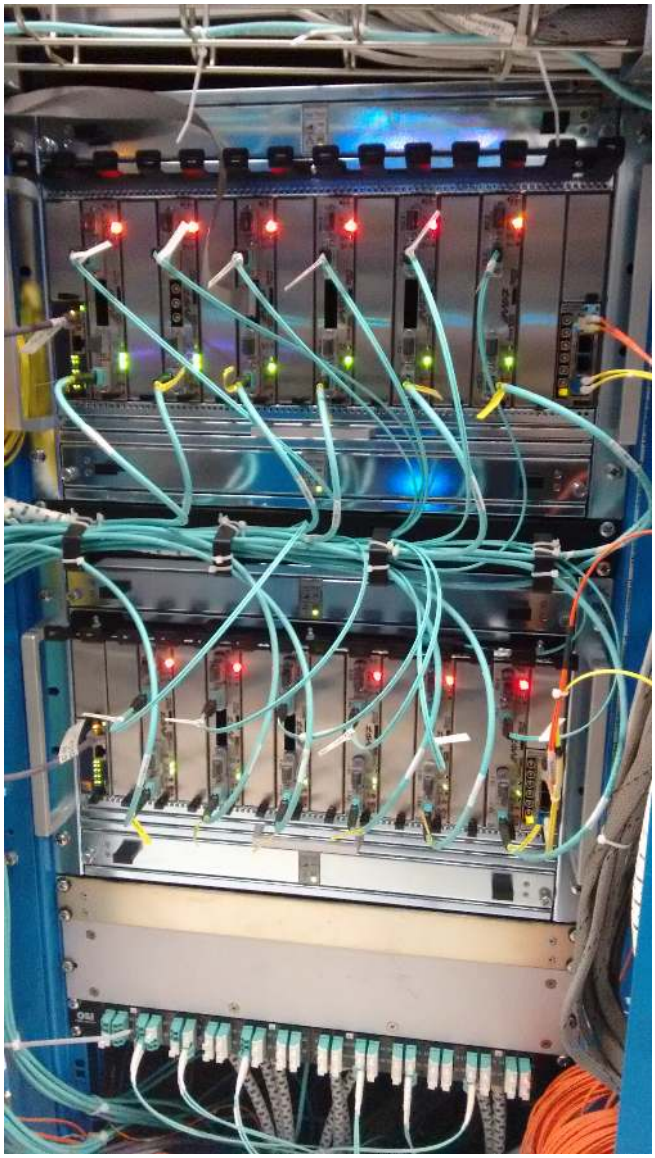


Figure 3.13: The BMTF system

The BMTF system is looking for muons within the pseudorapidity of $|\eta| < 0.83$. It receives muon super-primitives from the barrel distributed by the TwinMux system and synchronize the data of the same bunch crossing. It runs 144 ϕ-track finders in parallel (2 per sector x 6 per wedge[2] x 12 wedges) and choose the 3 best reconstruted muons per wedge which are finally sent to the next trigger system of the chain called μGMT. The protocol of both input and output links is commonly used in L1 Trigger and runs asynchronously at 10 Gb/s [2]. The heart of the MP7 is a *XC7VX690TFFG1927-2* FPGA, large enough to cover all requirements for the basic logic. The system is fully controlled by the IPbus which establish an Ethernet connection to a control PC in USC55 cavern. The BMTF during operation is monitored through IPbus and raises any system error or warning to the CMS control room.

BMTF is presented in details in chapter 4 as it is part of the main effort carried out in the present thesis.

[2]The track finders logically split the central sectors in two parts: + η and -η. Hence instead of 5 track finders the system runs 6.

3.1.2.4 Overlap Muon Track Finder (OMTF)

The OMTF is searching for muons in the common barrel-endcap region with 0.83 $< |\eta| <$ 1.24. The hardware platform of the OMTF is the Modular Track Finder virtex-7 (MTF7) dual board. The MTF7 (Figure 3.14) is used in both OMTF and EMTF systems. It consists of two AMC cards which are interconnected by a custom backplane [39]. The base card has two FPGAs: a Kintex-7, *XC7K70TFBG484-2* called Control FPGA and a Virtex-7 *XC7VX690TFFG1927-2* called Core FPGA. In addition it includes 1GB DRAM (RLDRAM) memory that is used to store large Look Up Tables (LUTs) with p_T values accessed by the track finder logic. The second card hosts the high-bandwidth optical links. The optical board is designed to receive 84 input links and 28 output links.

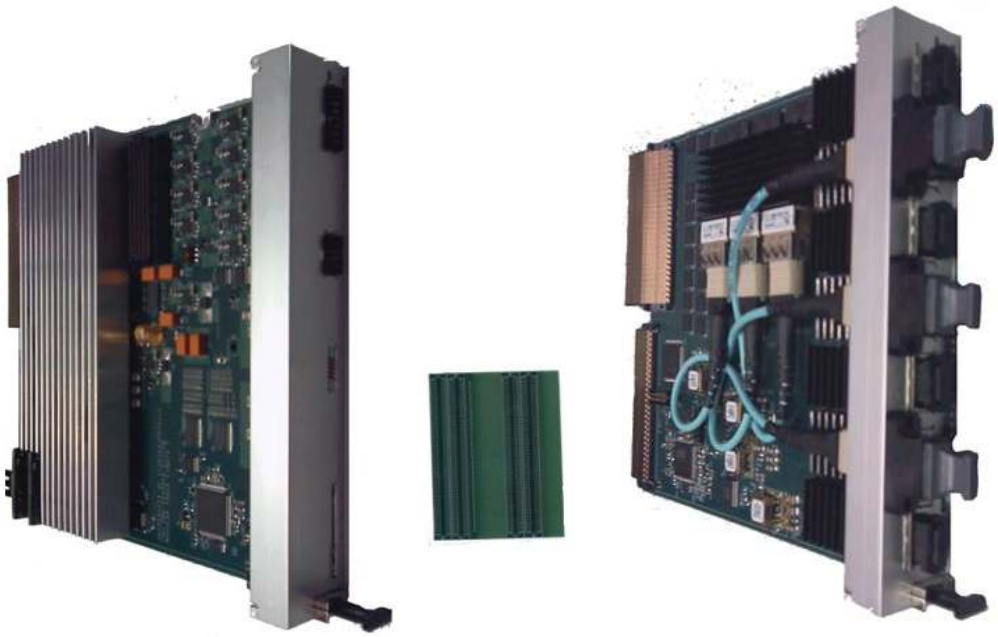


Figure 3.14: MTF7 dual board. On the left side is the optical board with the I/O links. On the right is the base board that hosts the virtex-7 Core FPGA. These are interconnected by a custom backplane (center).

The OMTF receives CSC inputs links at 3.2 Gb/s, synchronous with the LHC clock, and RPC - DT links at 10-Gb/s asynchronous to the LHC clock sent by the data concentrators (TwinMux and CPPF). The overlap region has a complex detector geometry and therefore the algorithm is based on the comparison of reconstructed signals from detectors with a set of precomputed patterns, called Golden Patterns (GPs). The GPs are objects that represent muon tracks with defined transverse momentum range and sign. The OMTF algorithm takes the advantage of the on board DDR3 memory of the MTF7 in order to store those p_T values. The OMTF analyzes the input primitives, identifies muon tracks and estimates their transversal momentum p_T. The system identifies and delivers up to 3 muon candidates per MTF7 for each bunch crossing. Each one for the 12 MTF7 modules, process data within 60° on each side of the two overlap regions and transfers the parameters to the micro Global Muon Trigger μGMT [40, 41].

3.1.2.5 Endcap Muon Track Finder (EMTF)

The Modular Track Finders virtex-6 (MTF6) and virtex-7 (MTF7) are AMC Boards used in the L1 muon trigger of CMS [39]. The Endcap Muon Track Finder, EMTF is based on the MTF7 to find muons that leave signals in the detectors of the encdap area $1.24 < |\eta| < 2.4$. The EMTF system collects data through optical links from both Cathode Strip Chambers, CSC and Resist Plate Chambers, RPC. In the first case a synchronous protocol running at 3.2 Gb/s is used to receive CSC data and in the second case an asynchronous protocol is used to receive 10-Gb/s RPC data from the CPPF data concentrator.

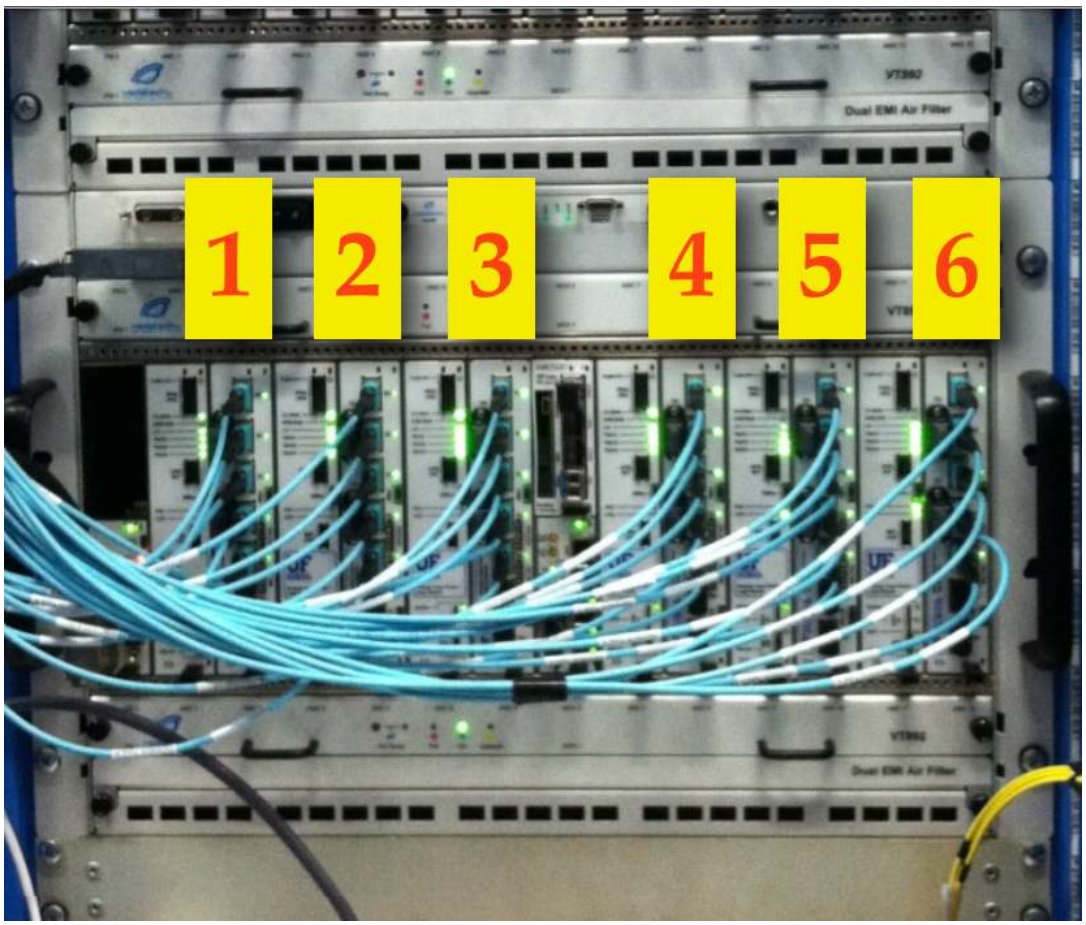


Figure 3.15: EMTF crate. It hosts six dual MTF7 modular platforms including one base card, one optical card and one LUT mezzanine. The optical cards are connected with multimode fibers operating up to 10 Gb/s.

The cards of the EMTF system are hosted in a μTCA Vadatech crates. Each crate (Figure 3.15) has six MTF7 boards (6 base + 6 optical modules), one Vadatech MCH, to access the MTF7 and control the crate [42] and one AMC13, to send triggered data to the EMTF FED and distribute the TTC clock and commands from the TCDS. The MTF7 hosts a mezzanine with a 1 GB RAM for loading the Look Up Tables (LUTs). This large memory is used by the algorithm to transform hit patterns to transverse momentum (p_T) values. Each one for the 12 MTF7 modules, process data within 60° on each endcap. Like the other Track Finders, each EMTF card sends the 3 best muons to the next stage through optical links running asynchronous 10 Gb/s protocol.

3.1.2.6 micro Global Muon Trigger

The old Global Muon Trigger, built using the VME standard, has been upgraded and replaced by the micro Global Muon Trigger μGMT. The prefix "micro" stands for the μTCA standard, used in all Level-1 Trigger systems after phase-I upgrade. The μGMT crate uses one MP7 board, one MCH and one AMC13 board. The MP7 of the μGMT receives data from the track finders using 64 input fibers (12 from BMTF, 12 from OMTF, 12 from EMTF and 28 from the CaloLayer2). In contrast to the old system, the upgraded Global Muon Trigger does not merge muons coming from the DT and CSC track-finders with those delivered by the RPC system, but it applies a final sorting algorithm in the three track finders and cancels-out duplicate muons found at the boundary between neibour track-finders. Finally, μGMT computes the isolation of a muon based on the energy deposited in the calorimeter Trigger Towers around a muon's track [4].

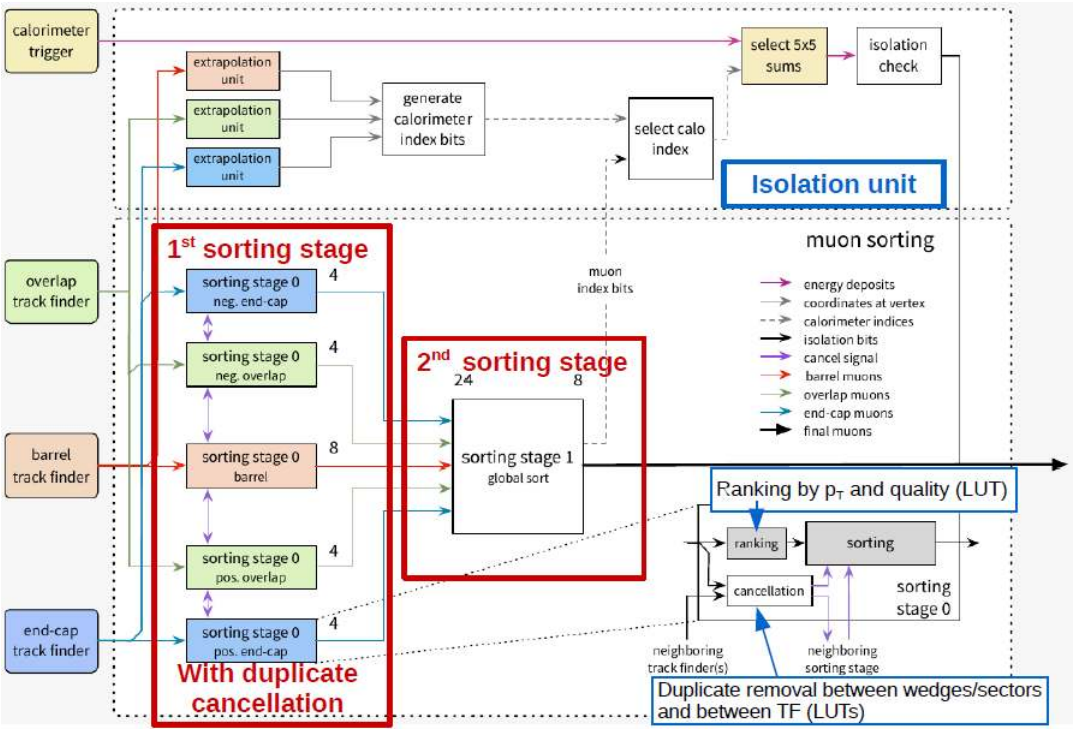


Figure 3.16: Logic block diagram of μGMT. The upper part shows the isolation unit and the lower part the sorting unit.

The lower part of Figure 3.16 shows the two muon sorting stages of the μGMT. In the first stage the muons from each track finder are sorted separately according to a rank assigned depending on the p_T and the track address of the muons. At the same time the algorithm finds and cancels ghosts (fake muons) by matching muon tracks in the boundaries. In the second stage, a sorter logic gets four muons from the positive and four from the negative regions of both the overlap and endcap track-finders, as well as eight muons from the barrel track finder. The best eight muons among the above 24 mouns are sent to the μGT. The upper part of Figure 3.16 presents the isolation unit. The value of the energy sum in the calorimeters at a given position is compared with a pre-defined threshold, to calculate the absolute isolation. The absolute isolation divided by the muon p_T gives its relative isolation.

Finally, the relative isolation values are merged with the sorted muons and sent to the μGT.

3.1.3 micro Global Trigger

An MP7 card is used in the upgraded Global Trigger (μGT) to perform the main algorithm of the Global Trigger. In addition, the AMC502 is used to consentrate and distribute LVDS signals from/to MP7 processors [43]. The AMC502 is a commercial card from Vadatech [44]. The block diagram of the AMC502 is presented in the Figure 3.17. The AMC502 hosts a large Kintex-7, *XC7K420TFFG1156-2* where the logic safely moves data from parallel LVDS signals to a 10-Gb/s serial link. AMC502 hosts an iMX6 which controls the card. A light linux OS (Fedora), accessed by the network, has been built in the card and uses the iMX6 CPU and the memories (Flash and DDR3) to allow the user to store and upload firmware to the AMC502 FPGA as well as develop software for testing. In addition, the card hosts an IPMI controller to check the status of sensors and request power from the backplane, a gigabit Ethernet switch to interconnect the FPGA and the Linux OS with the MCH of the μGT and a Phase Lock Loop (PLL) to distribute a low jitter clock to both FPGA, and CPU. A basic firmware designed for the AMC502 is presented in the Section 7.3.

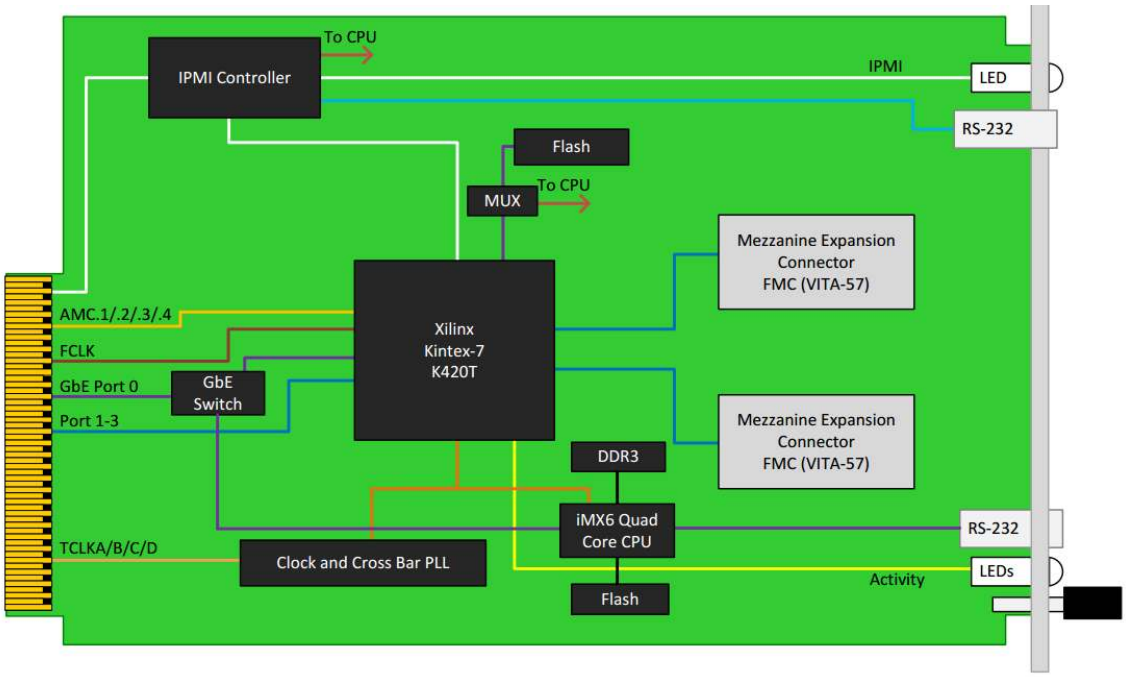


Figure 3.17: AMC502 block diagram.

The new μGT is the final link of the CMS L1 Trigger chain. It uses an asynchronous 10-Gb/s protocol to receive the inputs and recive more triggers objects than the old-trigger system: From the muon branch it receives 8 instead of 4 muon candidates and from the calorimeter branch it receives 12 electron/gamma objects instead of 8, 12 jets instead of 8, and 8 tau objects instead of 4. The μGT receives triggers from other CMS subdetectors and sources which are still connected to the old Global Trigger and called External Conditions (EC). Those signals are differential (LVDS) and therefore they are sent to the MP7 of the μGT via the AMC502 card.

As shown in Figure 3.18, four AMC502 on the right side of the crate are connected with 8 VHDCI (Very High-Density Cable Interconnect) cables that carry the ECs. The AMC502 synchronizes them and the output data are sent via an asynchronous 10-Gb/s link to the MP7 [45].

The MP7s (left side of the Figure 3.18) applies the trigger menu of the μGT system. It generates the Level-1 Accept (L1A) signal based on the inputs of the MP7 (muon triggers, calorimeter triggers and ECs). The VHDL code of the trigger menu is generated by software written in Python language. This software adopts the requirements for different physics conditions in the LHC and the CMS detector. The software's framework is a Graphical User Interface (GUI) that gives an easy access to the menu and stores the values in XML files [46]. The software uses those XML files to generate the algorithm part of the MP7 algorithm. As in the other trigger subsystems, the algorithm logic of the μGT is placed on top of the infrastructure logic in the processor's firmware.

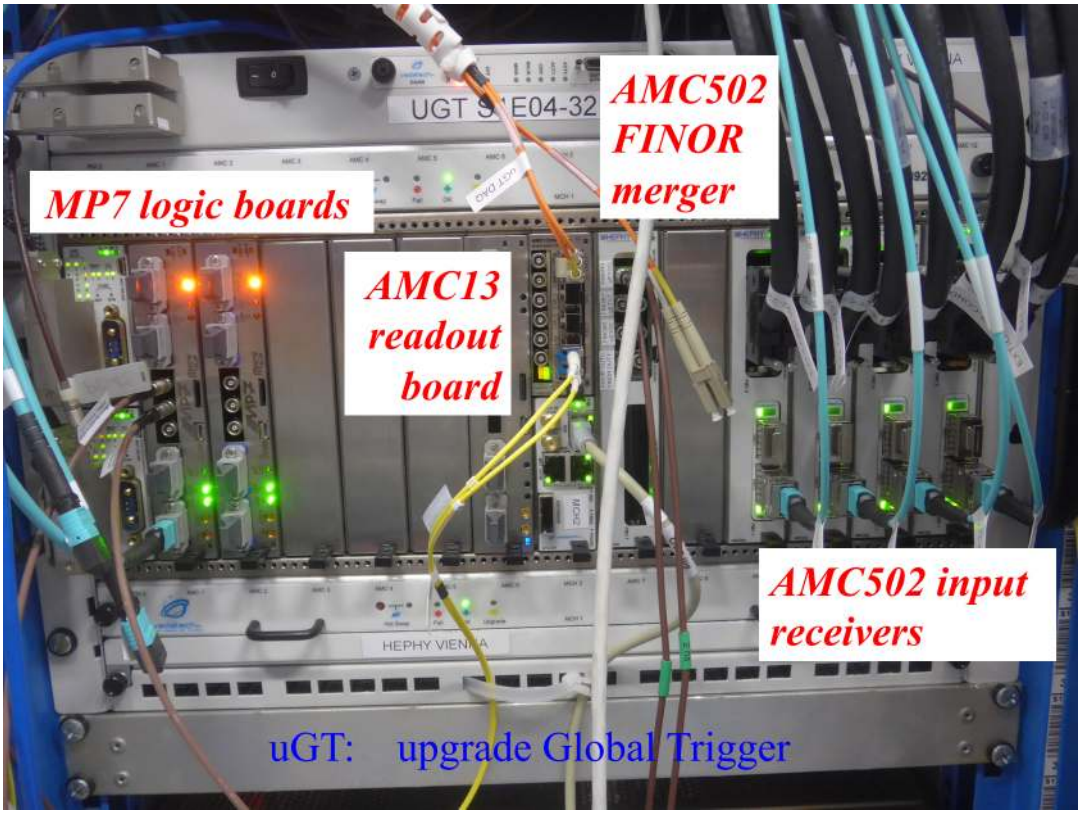


Figure 3.18: The μGT crate. From left to right the crate hosts two power modules, three MP7s (the first two are operational), one AMC13, one MCH and five AMC502 (the first generates the finalOR and the other four convert LVDS signals to 10-Gb/s asynchronous optical links).

The μGT algorithm logic is modular and if more logic is required it is foreseen to be extend in more than one MP7 processor. As the logic becomes more complex, the system is able to use up to 6 MP7s in parallel. The system delivers partial triggers to the AMC502 and this generates the so-called "finalOR" signal (FINOR). The FINOR (output of the μGT), is used as Level-1 Accept, triggers the readout of the detector and is used in the High Level Trigger system (HLT).

The central AMC502 (FINOR) of the crate receives the triggers of the old triggers

systems running in parallel using LEMO cables and low voltage TTL (LVTTL) input connections from the MP7s. In both sides mezzanine cards are installed in order to establish the connection. This 40 Mb/s connection has been chosen instead of an serializer/deserializer logic to avoid the increase of system latency.

3.2 The High Level Trigger

The second trigger level of CMS is called High Level Trigger (HLT) and is a software system implemented in a filter farm composed of commercial processors (13,000 CPUs). All high-resolution data from the detector readouts are stored in pipeline memories in the front-end electronics available to be processed by the HLT. The HLT aim is to reduce the trigger rate coming from the L1T about 1,000 times and deliver a maximum event rate of 100 Hz [47]. The HLT receives the information from the calorimeters and muon detectors to reconstruct physical objects. The event rate is reduced by applying requirements on the reconstructed objects properties. The HLT uses information from the pixel and strip detectors for track reconstruction and primary vertex identification [48]. The HLT algorithms are more complex and complicated than those of Level-1 Trigger which are implemented into FPGAs.

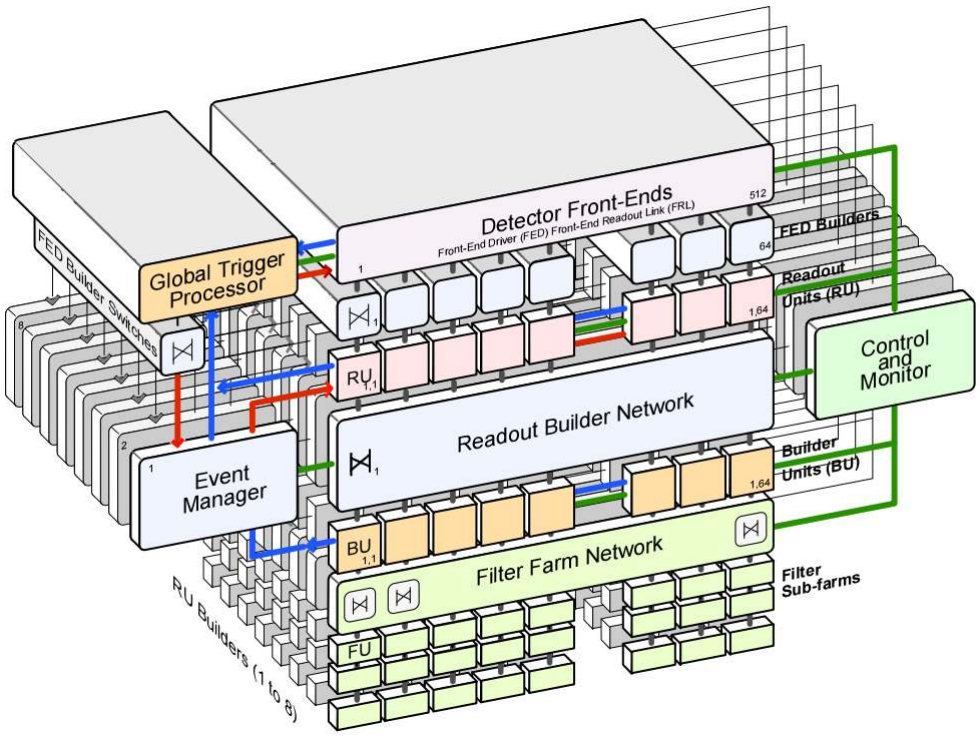


Figure 3.19: The event builder of the High Level Trigger (HLT).

The Figure 3.19 shows the event builder architecture. On the top are the Level-1 Trigger and the Detector Front-Ends.

Chapter 4

The Barrel Muon Track Finder

As described in Section 3.1.2.3, the Barrel Muon Track Finder (BMTF) searches for muons in the central region of CMS ($|\eta|$ <0.83). This region as well as the regions covered by the Overlap and Endcap Muon track Finders (OMTF, EMTF) are shown in the Figure 4.1. The BMTF receives DT and RPC information from all stations of the CMS barrel, except from the first layer of the outer wheels.

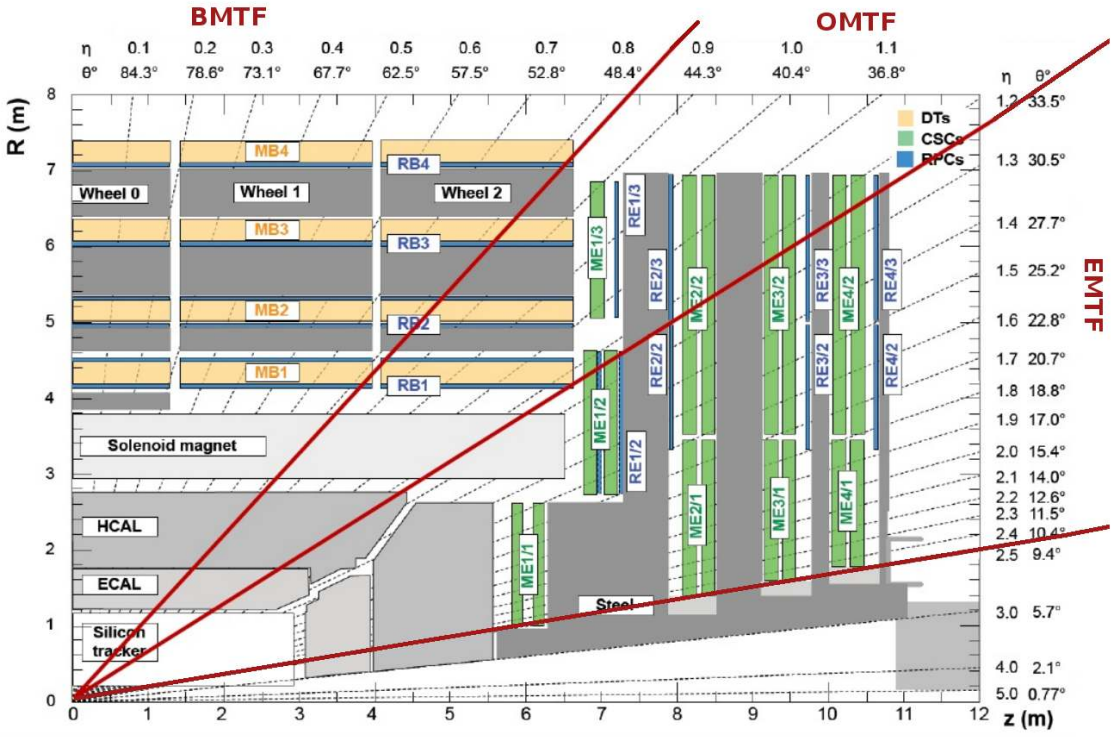


Figure 4.1: The longitudinal view of one quarter of CMS detector and the three muon track finder regions: BMTF, OMTF and EMTF.

The BMTF identifies muons tracks after processing detector's raw data (trigger primitives). These data are generated by the on-detector electronics and contain information about muon candidates for each of the four muon stations within a sector. This information includes position (η and ϕ coordinates) as well as bending

in ϕ coordinate (ϕ_b). The information is accompanied by quality bits that express the way the front-end electronics form the trigger primitives. The ϕ quality bits give the correlation of trigger primitives between the Super Layers of the detectors whereas the η quality 21 bits determine if the information hits are false or true. ϕ is 12-bits long, and ϕ_b 10 bits. Both are given in 2's complement format which leads to range of -2,048 to 2,047 and -512 to 511 respectively and η is 7-bit long (Appendix B).

The trigger primitives of one muon candidate are delivered by one 10-Gb/s optical link i.e. 192 bits at the bunch crossing frequency (BX). Each BMTF card processes two muons per DT sector and thus receives the data using two links per sector. Each BMTF Advanced Mezzanine Card (AMC) card is searching for muons within one barrel wedge. It receives the trigger primitives from its own wedge as well as from the neighbor wedges. Therefore 3 wedges use 30 optical links.

Each processor finds up to 3 best muons per wedge and sends them to the micro Global Muon Trigger (μGMT) using one optical link. The muon information is: p_T (9-bits), quality (4-bits), pseudorapidity (9-bits), azimuth angle (8-bits) and track address (14-bits). The p_T scale is linear with stepsize of 0.5 GeV. The range is 3 to 140 GeV. In addition pseudorapidity scale is linear and η is encoded in 2's complement format in the range -230 to 230 in steps of 0.010875.

4.1 The BMTF algorithm

The logic blocks of the BMTF algorithm are presented in the block diagram of the Figure 4.2. The BMTF system receives muon-trigger primitives from the detectors through serial optical links. After the deserialization stage, the data frames are aligned in respect to the bunch crossing ratio (40.08 MHz) and enter the three branches of the algorithm:

1. The ETA Track Finder branch (ETTF) of the algorithm is pipelining the trigger primitives in order to synchronize the η-matching block output with the track linker unit output of the PHI track finder (next branch). ETA matching unit correlates η from the different η stations within one sector. The ETA selection unit uses the track address found by the PHI track finder to select one of the eta tracks found. The result of the ETTF is delayed to be synchronized with the output of the Assignment unit.

2. The PHI Track Finder (PHTF) uses an extrapolation mechanism to identify muons trajectories from their track segments within one sector. Partial trajectories from all neighbor sectors are forwarded to the track linker unit in order to form one unified trajectory.

3. The Assignment Unit pipelines the trigger primitives until the track addresses are generated. Then it uses the track addresses to select the corresponding trigger primitives. Finally, the selected data primitives are used as inputs of LUT in order to assign the parameters to the muons found.

The above algorithm runs on each card (one wedge) 12 times in parallel and it provides all the physical information of the muon candidates (p_T, ϕ, η). Before

selecting the 3 best muons the algorithm checks for identical track addresses in order to find trajectories that refer to the same muon. In case it finds two trajectories with similar track addresses it cancels-out the one with the shorter track. Finally, the processing unit compares the found muon candidates in order to choose those with the highest transverse momentum. Then it forwards the best of the them to the next system in the trigger chain (μGMT).

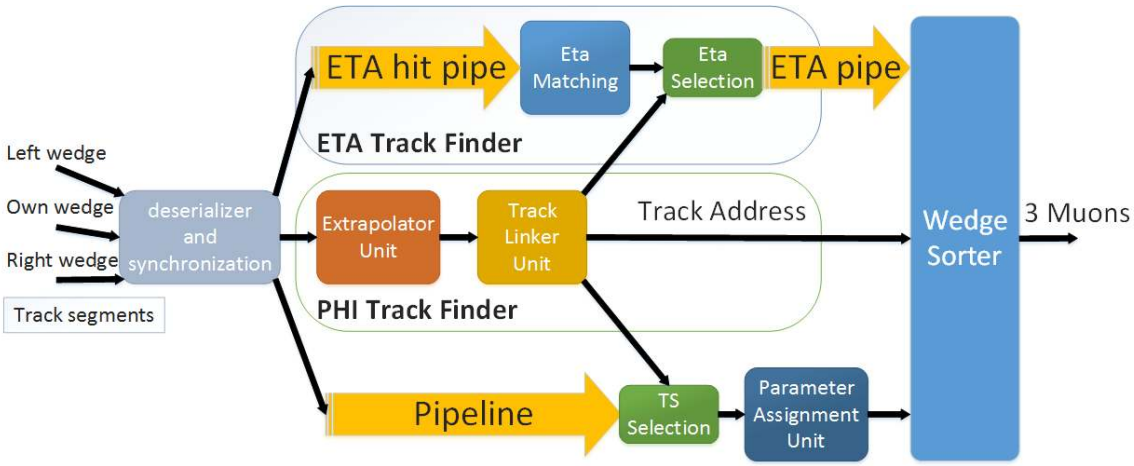


Figure 4.2: Block diagram of the track finder algorithm.

4.1.1 Input and synchronization

Each BMTF processor card receives 30 links from one reference wedge and its two neighboring wedges (10 each). These links are grouped in pairs and the 15 muons sectors of 3 wedges are connected to one BMTF card. Appendix B describes the input channel allocation to the BMTF card.

Each "deserialization and synchronization" unit receives 2 links corresponding to 6 x 32-bit words each in the 240-MHz clock domain. This unit delivers totally 384 bits in the clock domain of the algorithm (160 MHz). The unit applies programmable quality thresholds which are available for testing. Also it generates input data flags used in the monitoring blocks. Finally, it finds the correlated trigger primitives information that is used later in the parameter assignment unit.

4.1.2 PHI Track Finder

The PHI Track finder is the main brunch of the algorithm. It defines the presense of a muon track and gives the muon-track information to the other two branches of the algorithm. It uses extrapolation Look-Up Tables to find partial muon trajectories which it uses to reconstruct track addresses and finally, assign the physical parameters of the track. The block diagram of the PHI track finder is shown in Figure 4.3 [2, 49, 27].

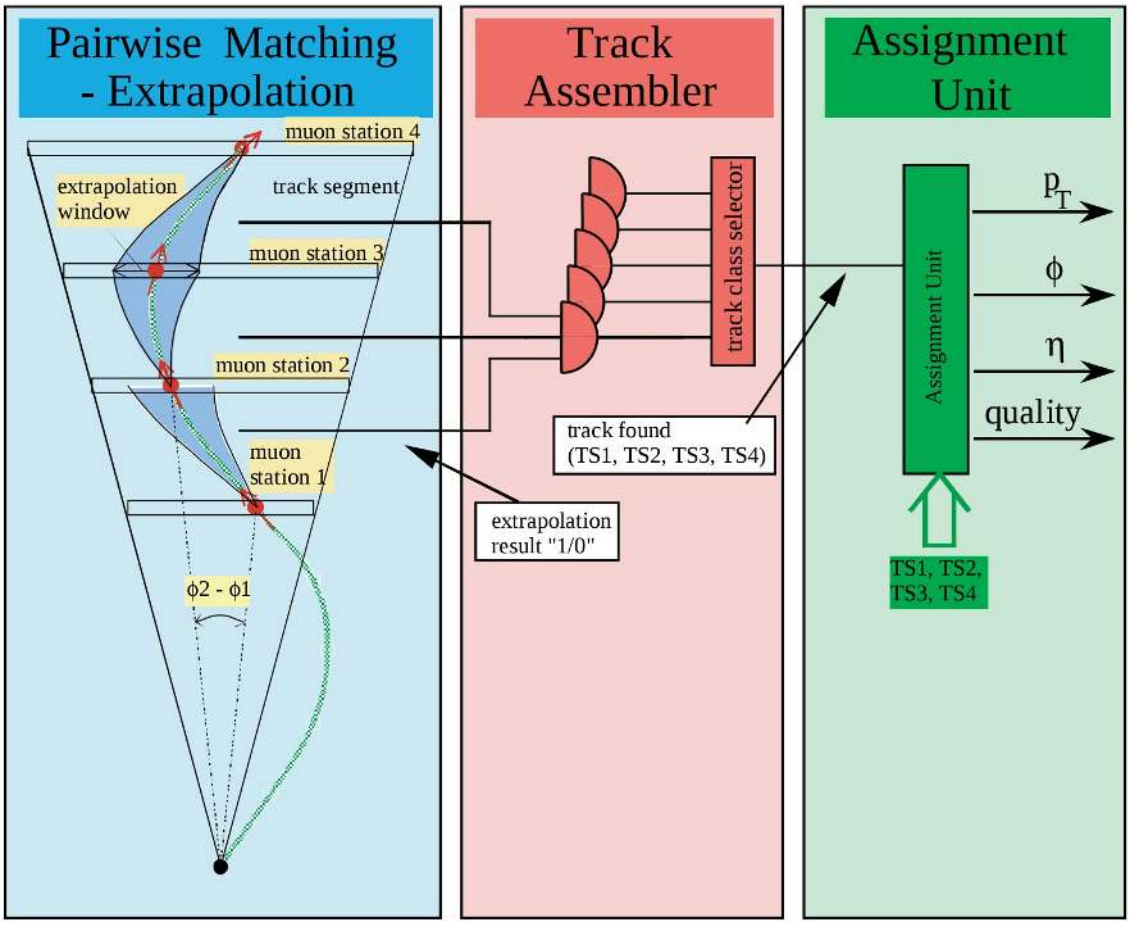


Figure 4.3: PHI Track finder and assignment unit

4.1.2.1 Extrapolation unit

The fundamental function of the BMTF algorithm is the reconstruction of a muon track when the muon hits two neighboring DT stations. One of the stations is defined as the source station and the other as the target station. The extrapolation is applied from the source to the target station resulting to a ϕ and a ϕ_b coordinate on the target. The ϕ coordinate of the extrapolation is defined by the equation 4.1 and is equal to the sum of the source ϕ and its deviation due to the bending (ϕ_b). The deviation is assigned using FPGA memories which are called extrapolation Look-Up tables: $\phi_{deviation}(\phi_{b,source})$.

$$\phi_{extrapolated} = \phi_{source} + \phi_{deviation}(\phi_{b,source}) \tag{4.1}$$

If the $\phi_{extrapolated}$ is below a threshold (equation 4.2) the track between the two DT stations marked as acceptable. In Figure 4.4 the extrapolation from the source station (inner) to the target station (outer) is shown.

$$threshold_{extrapolated} \geq |\phi_{extrapolated} - \phi_{target}| \tag{4.2}$$

DT sector has 4 stations (MB1, MB2, MB3 and MB4). Thus the extrapolation is running in parallel for the pairs MB1→MB2, MB1→MB3, MB1→MB4, MB2→MB3, MB2→MB4 and MB4→MB3. Extrapolation on the two outer stations (MB3, MB4)

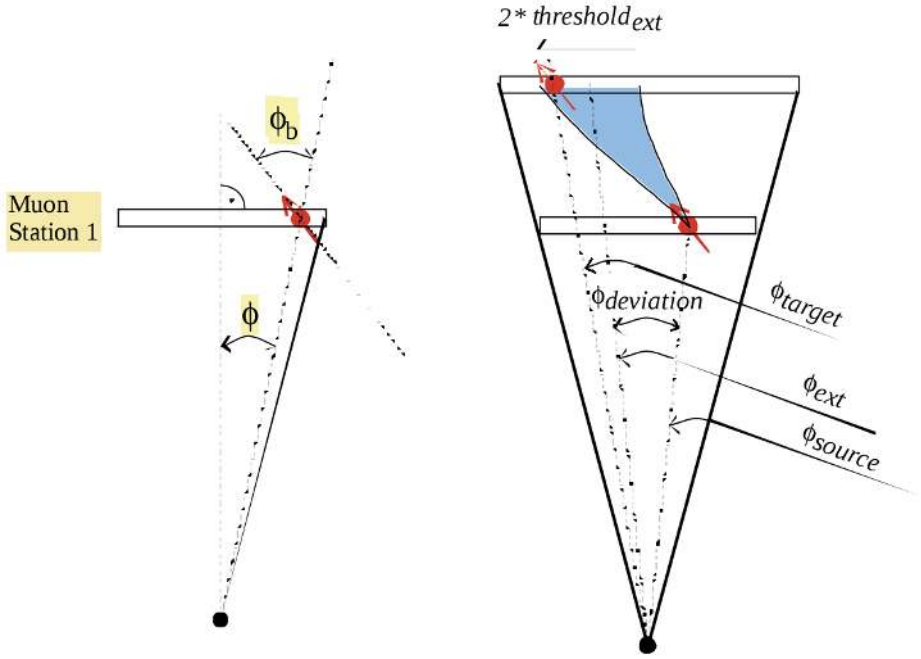


Figure 4.4: Extrapolation parameters. Left: ϕ and ϕ_b angles, right: ϕ_{source}, $\phi_{extrapolated}$, ϕ_{target}, $\phi_{deviation}$ and the acceptable window.

is running backwards because the muon energy loss at the third station results to a small bending angle that renders the extrapolation unpredictable.

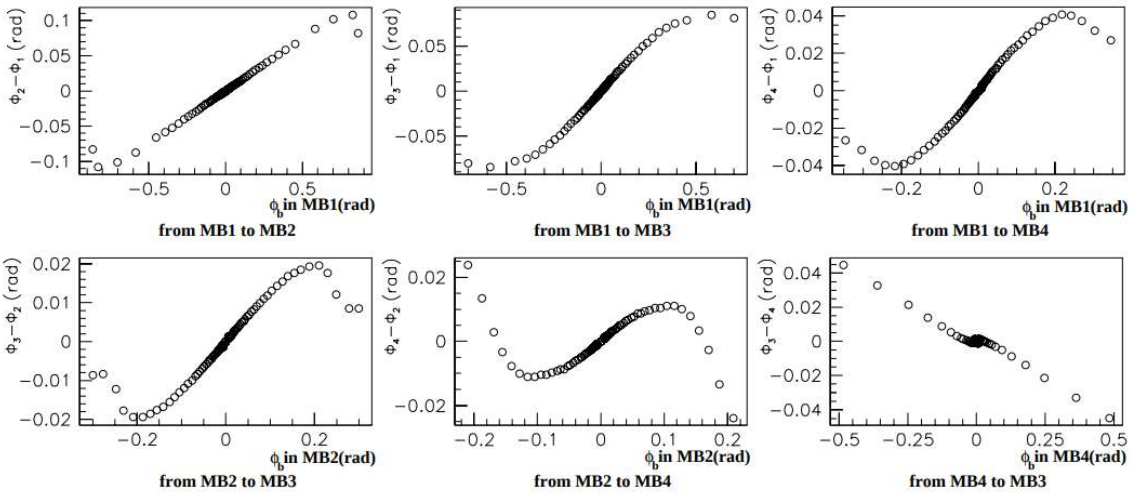


Figure 4.5: Deflection of a muon track ϕ_{target} - ϕ_{source}, for all Muon Station pairs as a function of the bending angle $\phi_{b,source}$

Due to their bending in ϕ and their direction in η, muons can cross neighbour sectors. To cover those cases, the extrapolation unit is running in addition to the main sector in parallel on the neighbour sectors. Thus each BMTF processor card runs the algorithm for one detector wedge and its neighbors.

Figure 4.6 shows red dots with arrows that point to stations on certain sectors and all possible combinations of extrapolation. The algorithm is applied in parallel. The 6 PHI Track finder instances and one ETA track finder are written in VHDL. Since the muon candidate is produced in the center of CMS and due to the magnetic field, its trajectory starts from the center and can travel through DTs of one or two neighbour sectors. To cover all possible tracks the algorithm is applied in multiple times as shown in Figure 4.6. The wheel 0 is logically spit in two parts: negative and the positive side of wheel 0 (+0 and -0). As an example, the Track finder of the sector in wedge 6 and wheel -1, processes track segments from one of the stations that belongs to the sector 6 (called *own sector*) as well as track segments from the stations belonging to the same of neighbor detectors (wedge 5, 6, 7, wheel -1, -2). Then the PHI track finder calculates an extrapolation of one inner station to each of the outer stations of wheels -1, -2 and wedges 5, 6, 7.

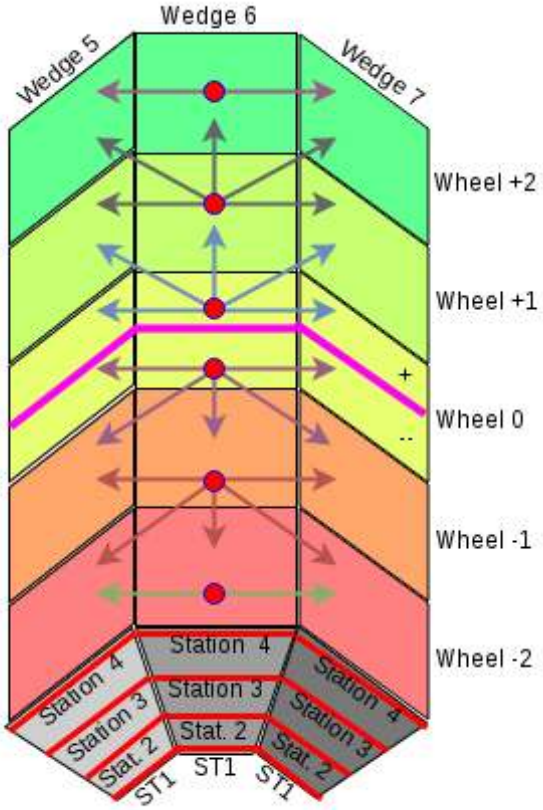


Figure 4.6: One detector muon wedge (wedge 6) in which trigger primitives are processed by 6 PHTFs (showing in red dots) in order to find possible partial muon tracks (arrows).

4.1.2.2 Assembler unit

The algorithm links partial trajectories to create a muon track candidate. The matching station pairs found by the extrapolation unit are linked together and the result is assigned by its track address. The track address is a 14-bit word that encodes the presence of the first or the second acceptable muon track (TS1, TS2) for each sector. The first two bits of the track address are referring to the first station and the rest three parts of four bits are referring, to the 2nd, 3rd and 4th stations.

Track Address: 14bits = 2bits (St.1) + 4bits (St.2) + 4bits (St.3) + 4bits (St.4)

If all bits of a track address within a station are high ('1'), no acceptable muon candidate exists in that station. The track address of the first station has only two bits since it carries less information than the outer stations and therefore can get the hexadecimal values: 0x2 (TS1), 0x1 (TS2) and 0x0 (Null). The other stations can get the hexadecimal numbers: 0xa, 0x8, 0xc, 0x2, 0x0, 0x4 (TS1), 0xb, 0x9, 0xd, 0x3, 0x1, 0x5 (TS2) and 0xf (Null) according to their relative track finder wheel and sector. The encoding format of the track addresses is given in Table 4.1.

	Reference Wheel			Next Wheel		
	TS1	**TS2**	**Null**	**TS1**	**TS2**	**Null**
Left Sector	0xa	0xb	0xf	0x2	0x3	0xf
Reference Sector	*(0x2)*0x8	*(0x1)*0x9	*(0x3)*0xf	0x0	0x1	0xf
Right Sector	0xc	0xd	0xf	0x4	0x5	0xf

Table 4.1: Track address encoding (hex format). Within the parenthesis the first station values are shown.

Figure 4.7 shows one PHTF algorithm instance running over 1 sector and its 5 neighbor sectors. Each station is shown as a rectangular which is accompanied by 5 neighbor rectangulars all grouped as MB1, MB2, MB3 and MB4 stations. They are divided in OWN sectors indicating that belong to the wedge of the own PHTF algorithm instance, in LEFT indicating the counter-clockwise PHTF and RIGHT the clockwise PHTF in ϕ. Respectively to the right and left division, the sectors are divided also in OWN and NEXT wheel. OWN wheel indicates PHTF algorithm instance of the same wheel and NEXT the PHTF instance of the next wheel (higher value of $|Z|$ coordinate or $|\eta|$). The numbers are the address given to muon track when the muon is identified from the BMTF algorithm.

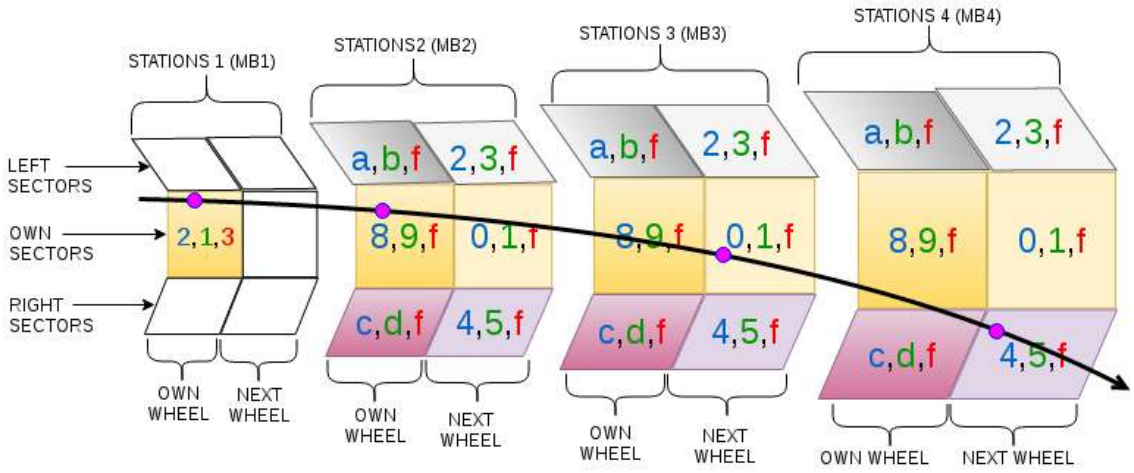


Figure 4.7: A muon that gives the track address 0x2804. This muon leaves signal in own sector - own wheel - station 1, own sector - own wheel - station 2, own sector - next wheel - station 3, right sector - next wheel - station 4. In this example the track segments are exclusively from the TS1.

4.1.2.3 Assignment unit

This unit uses the trigger primitives of triggered muons to assign the physical parameters to them. First, all trigger primitives of the BMTF are pipelined until the assembler unit extracts the track address. Then the track addresses are used to select the trigger primitives that belong to the found muons. The assignment is done using precalculated values that are stored for specific inputs. These precalculated values are stored in Look-Up Tables in FPGA memories, and are used to give the transverse momentum (p_T), phi angle (ϕ) and quality bits to the reconstructed muons. During

the trigger upgrade phase I the parameter assignment block of the BMTF has been improved compared to the old DTTF system.

In particular, and contrast to the old system in which the assignment of the p_T was done by using 5-bits ($2^5 = 32$ different p_T values), the BMTF uses 9-bits which gives a number of $2^9 = 512$ different values. This increment of the dynamic range of the p_T is one of the benefits that the new powerful hardware offers to the system. In Appendix C, the output definition of all the parameters of the BMTF are presented.

The new assignment algorithm is based on ϕ_b trigger primitives of the inner station rather than $\Delta\varphi$ between the inner and the outer stations used in the old algorithm. In order to implement the new assignment algorithm, additional LUTs and logic (showing with purple color in Figure 4.8) are implemented in the FPGA. This new algorithm runs in parallel with the old one and gets priority under two conditions:

1. The track segments are defined as correlated by the DT front-end electronics. In the BMTF, correlated is a track segment with data quality equal or higher to 3.

2. The p_T output of the old algorithm is smaller than the p_T output of the new algorithm.

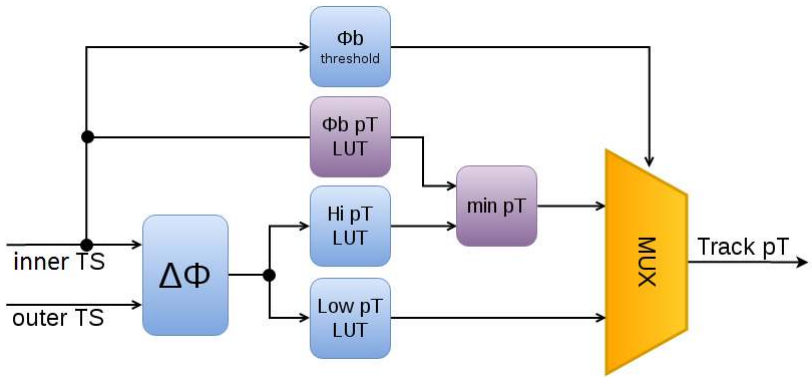


Figure 4.8: The assignment algorithm. The blocks in blue are parts of the old algorithm and in purple of the new algorithm. The p_T assignment is calculated either using the ϕ difference between the inner and the outer stations or by the ϕ_b of the inner station.

4.1.3 ETA Track Finder

The ETA Track Finder (ETTF) runs over one wedge of the DT barrel. Each of the 5 sectors of the wedge accommodates 3 ETA stations and each station contains 7 consecutive chamber areas (Figure 4.9). ETTF receives 14-bits per ETA station. Each pair of bits is assigned to a chamber area as 1 "hit" bit and 1 "quality" bit. The "hit" bit indicates whether there was a hit in the area and the second one gives the quality. If all four planes of an η superlayer are hit, the hit bit and the quality bit are assigned to logical '1'. If only three out of four planes are hit, the hit bit is set to '1' and the quality bit to '0'. If fewer than three planes are hit, both are

assigned to '0'. ETTF compares the hit pattern with predefined track patterns. After matching with predefined track patterns, the ETTF tries to match the η-track with ϕ-tracks found by the PHTF. If the matching is successful, a precise value is assigned as *fine-η*. The matching mechanism is performed by categories that occur from different the track addresses. If the matching fails *rough-η* value is assigned to the triggered muon. The ETTF output is pipelined in order to delivered to the wedge sorter in time with the output of the parameter assignment unit. The WS can therefore process them as a single entity.

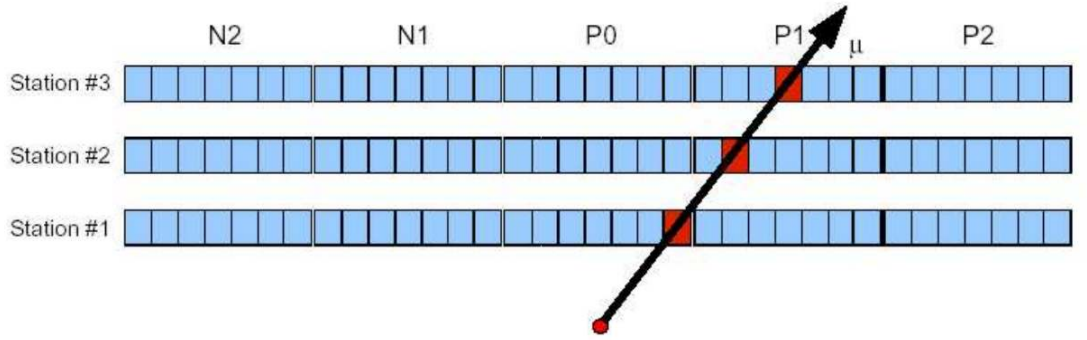


Figure 4.9: In a wedge of the muon chambers a muon hit: the seventh area of the station 1 in wheel 0, the second area of station 2 and the forth area of station 3 in wheel 1. N2, N1, P0, P1 and P2 are sectors.

4.1.4 Muon sorter and cancel-out

The muon sorter is the final stage of BMTF algorithm. Is taking place before the system serializes the data and transmits them via optical links to μGMT. Data of all PHTF and ETTF instances are concentrated and assigned to the wedge sorter as objects having p_T, quality bits, ϕ, η and track addresses. The unit first finds any duplicate muons, cancels-out the "ghosts" and then sorts the selected muons according to their p_T. The cancel-out procedure is based on the track addresses of the muons using the following mechanism: If the track finder of the "own" wheel station finds a track address that corresponds to the next wheel station and the track finders of the next wheel station find a track address in its "own" wheel station, that means that the same muon has been found twice and one of them is a "ghost" muon. The cancel-out (called also muon ghost-busting) depends on the quality bits and the muon with the lower quality is canceled. The Table 4.2 shows the track addresses of the own and next wheel stations that enable the muon cancel-out mechanism.

	Left wedge		Own wedge		Right wedge	
	TS1	TS2	TS1	TS2	TS1	TS2
Own wheel	0x2	0x3	0x0	0x1	0x4	0x5
Next wheel	0xa	0xb	0x8	0x9	0xc	0xd

Table 4.2: Cases with two found muons including a ghost muon.

Each track finder searches for 2 muons in 6 PHTFs (as have been explained in Subsection 4.1.2.1) and thus can find up to 2 x 6=12 muons. The 3 best of the 12

muon candidates are selected to be sent to the μGMT Trigger system. The primary muon-sorting criterion is their p_T and the secondary their quality as recorded in the respective bits. The 3 track canditates ranked higher than the rest are kept. The final muon sorting and "cancel-out" is done in the next trigger system, the μGMT [4], which rejects duplicate muons between wedges and selects the 4 best muons out of 36.

4.2 System architecture

The BMTF firmware implemented on a Master Processor virtex-7 (MP7) card searches for muon tracks within one wedge, running in parallel 6 PHTF algorithms. As shown in Figure 4.10, each wedge is sharing information with its neighbor wedges. For instance trigger primitives from sector 2 are shared between wedge 1, 2 and 3, in order to provide information for muons that cross neighbor wedges. According to the phase 1 trigger upgrade the data sharing is done by the new sector collector called, TwinMux. The TwinMux concentrates DT and RPC trigger primitives and creates the appropriate fan-out to serve the BMTF sharing links [3, 2].

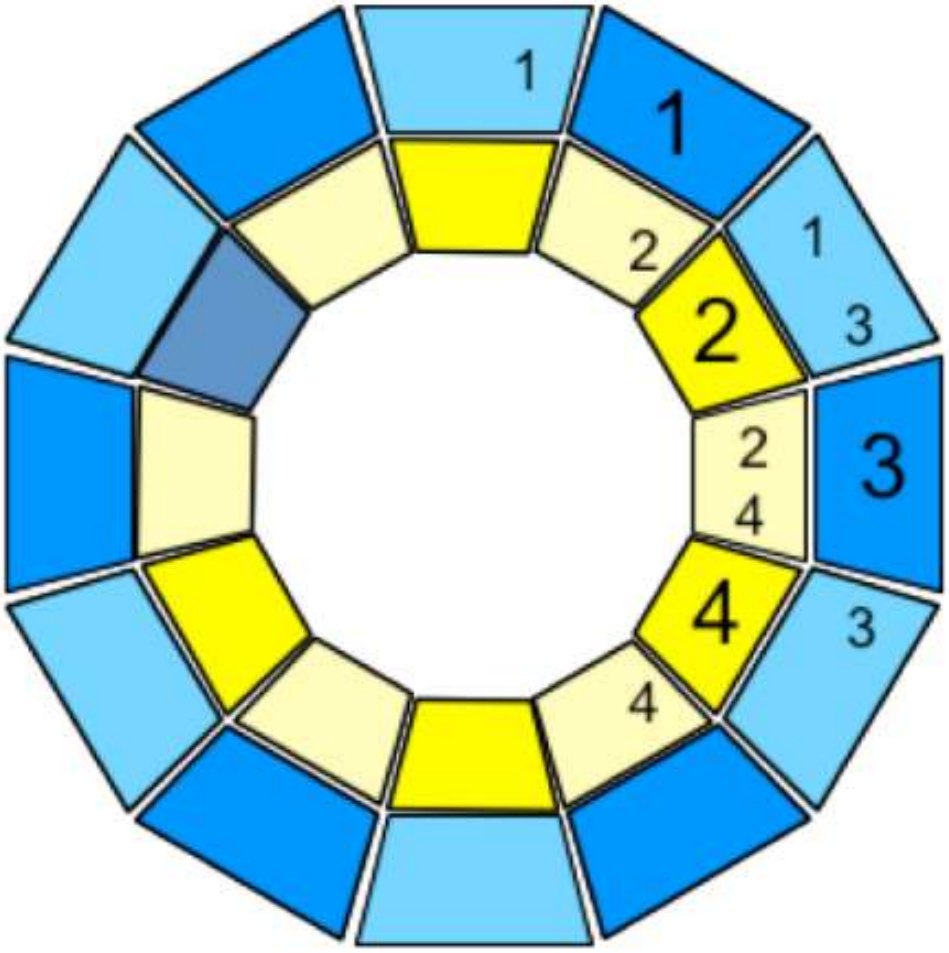


Figure 4.10: The partitioning and data sharing of the BMTF. The design employs in total 12 processors.

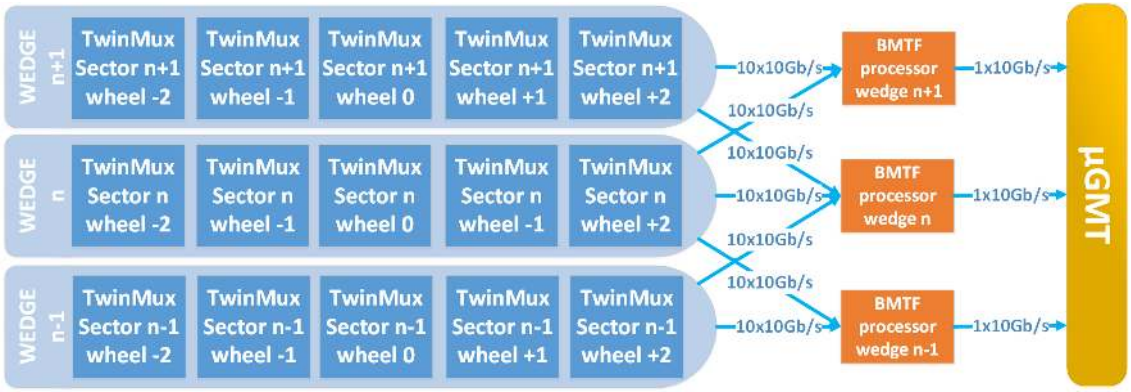


Figure 4.11: Distribution of input data primitives to the BMTF processor and output triggered data from the BMTF processor. With blue color the Twinmux cards, with orange the BMTF and with yellow the μGMT (both MP7s) are shown.

Each BMTF MP7 card is capable to process all information from one muon wedge and run the corresponding ϕ and η track finders. Since the CMS has twelve wedges, the same number of BMTF MP7 processor cards are used. As shown in Figure 4.11, the BMTF processor number n, receives the data primitives using optical links (blue color arrows) form wedges n, n-1 and n+1. Subsequently, the BMTF processor collects the information from three wedges using 30 links running at 10 Gb/s i.e. a bandwidth of 300 Gb/s. The output of BMTF is sent using one 10-Gb/s link to the μGMT.

Figure 4.12: Left: 360 LC optical links are connected to the TwinMux patch panel carrying muon primitives to 12 BMTF processors (MP7 cards, right). Right: Each of the 12 trunk cables carries 30 LC links (12x30=360 overall) and is connected to the input of each of the 12 MP7s.

As shown on the left side of Figure 4.12, 12 MTP trunk cables with 30 LC channels are connected to the TwinMux patch panel. The total BMTF bandwidth is 12 (cables) x 30 (channels) x 10 Gb/s (data rate) = 3.6 Tb/s. On the output the BMTF uses the same transmission protocol as in the input. One link per processor sends the BMTF results to μGMT. One additional output link duplicates the output to the μGMT for redundancy reasons. As can be seen on the right side of Figure

4.12, the BMTF uses two μTCA crates that host twelve BMTF processors. It has been chosen to divide the system into two half-barrel crates which organize these processors on top and bottom card as shown in Figure 4.13. The split is done due to the limited available bandwidth provided by the DAQ system (10 Gb/s) and due the lack of zero suppression[1] procedure in the BMTF.

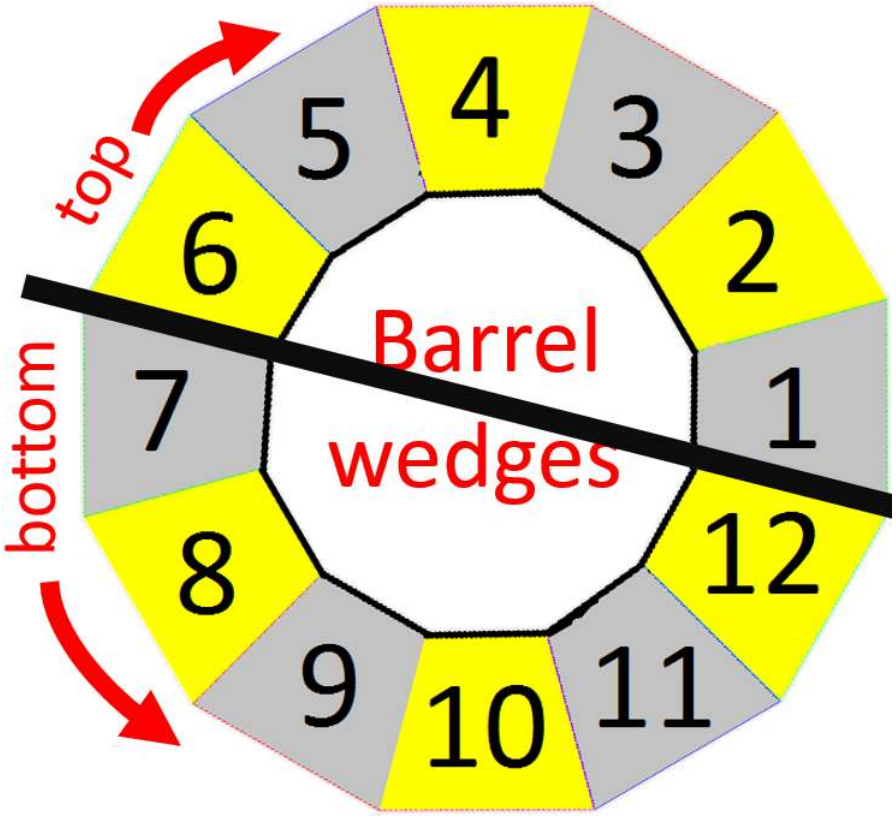


Figure 4.13: The BMTF system is splitted into two crates. The TOP includes the 1, 2, 3, 4, 5, 6 processors and the BOTTOM the 7, 8, 9, 10, 11, 12.

The available DAQ bandwidth is set by the data throughput of the optical links used by the DAQ hardware in the μTCA crate. This hardware is called AMC13. Its DAQ link bandwidth is 10.3125 Gb/s, and sends the BMTF data to the trigger Front End Driver (FEDs) when it receives the L1A signal. Taking into account the data rate and the 64b66b encoding used by the protocol, the payload (together with header and trailer) is 8.96 Gb/s. Hence after phase 1 trigger upgrade the actual DAQ data throughput per μTCA crate is about 8 Gb/s. The event size of the BMTF system is calculated as:

$$32\ bit \times 6\ frames \times 5\ BXs \times (10\ input + 1\ output) \times 12\ MP7s = 16\ KB$$

The BMTF event size is calculated taking into account the number of I/O bits per BX (32 bits x 6 frames), the bunch crossing window (5 BXs), the total number of I/Os links of the own wedge (10 inputs + 1 output) and the number of the processor cards (12 MP7s). This event size can be served by splitting the BMTF system in two crates as explained above. Then one optical link per BMTF crate can cover the required throughput.

[1]Zero suppression concerns the DAQ data-flow and is the rejection of non-triggered events.

The required BMTF bandwidth per BMTF crate is calculated as:

16 KB × 100 KHz / 2 (crates) = 6.4 Gb/s < 8 Gb/s

where the event size is multiplying with the maximum L1A rate (100 KHz). After the BMTF was installed, the maximum trigger rate was increased to 150 KHz and the required bandwidth has been increased to 9.6 Gb/s and the optical links were not enough.

In addition a fixed suppression factor of 107 on selected bunch crossings has been applied. BMTF applies this suppression on -2, -1, 1 ,2 BXs and leave 0 BX suppressed. The new event size is:

32 bit × 6 fr. × (1+4/107) BXs × (10 input + 1 output) × 12 MP7s = 3.2 KB

Multiplying the event size with the new maximum trigger rate gives a low required bandwidth:

1.6 KB × 150 KHz / 2 (crates) = 1.92 Gb/s < 8 Gb/s

Which can be served by one DAQ optical link. Nevertheless, the setup was remained unchanged since it was stable and therefore two optical links are in use for DAQ.

4.3 Hardware architecture

The BMTF as all the other Level-1 Trigger systems uses the μTCA standard after detailed studies made at CERN [50, 51]. In particular the BMTF Schroff MicroTCA.4 crate is used [52]. This is a 9U crate, capable to host 12 double full-size AMC modules, 4 single-size-power modules [53], 2 MicroTCA Carrier Hub (MCH) single-size modules and fans whose speed is adjusted via the MCH.

Figure 4.14: The BMTF TOP crate.

The two BMTF crates follow a common scheme (hardware and fiber) for the interconnections. The top crate is shown in Figure 4.14. On the left side a commercial NAT-MCH module has been installed [54]. The MCH reads the status of the hardware sensors and distributes the power to the AMCs. Moreover, it gives access to all

modules via Ethernet and provides an interface to the user (telnet, web, serial etc). On the right side of the crate the AMC13 is mounted. This single-size AMC took its name from the fact that is used as the 13th AMC card exists in all the μTCA crates at CMS. The AMC13 provides Timing, Trigger and Control (TTC), Data Acquisition (DAQ) and Trigger Throttling System (TTS) services to the modules in the MicroTCA crate for CMS [55]. It occupies the second redundant MCH slot. In particular, receives and decodes commands from the TTC fiber (the bottom fiber shown in the AMC13 of the Figure 4.14) and sends the status of the system to the Trigger Throttle System (TTS) [56]. From the same fiber it distributes the LHC clock (40.08 MHz) and the Level1-Accept (L1A) on the μTCA CLK1 backplane line. The AMC13 uses the other fiber (the top fiber, mounted to the AMC13 of the Figure 4.14) to establish a connection with a Front-End Driver (FED) using 10.3 Gb/s optical fiber. The AMC13 requests triggered data from the readout buffers of the on crate AMCs when it gets the L1A from the TCDS. Then it organizes the data in packets adding headers and footers and sends them to the FEDs.

4.3.1 BMTF processor - MP7

As mentioned in Section 4.2, the BMTF relies on its wedge processors. It uses the Master Processors virtex7 (MP7s) as it provides a large (*XC7VX690TFFG1927-2* part) Virtex-7 FPGA excellent wrapped by hardware components that deal with [32]:

- 72 I/Os high-speed links (up to 12 Gb/s). MP7 has 6 transmitter and 6 receiver minipod modules from Avago Technologies, each providing 12 optical links. Minipods offer a compact and modular solution which allows 36 links from 3 minipods to be connected to one MTP connector mounted in the card's front panel. Also minipods give the flexibility to be replaced in case of a malfunction.

- 32-bit Atmel microcontroller (AT32UC3A3) that implement the Intelligent Platform Management Interface (IPMI) interface. IPMI is a part of μTCA specification and manages the AMC card powering, status and control.

- Storage of firmware bitfiles using an micro Secure Digital (μSD) card. The μSD is connected to the on board Atmel microcontroller which receives the data stream from the FPGA and stores it to the μSD. The firmware bitfiles are uploaded via Ethernet connection thought the FPGA and the controller to the μSD.

- DC/DC converters from Linear Technology that use the μTCA power to provide the power to the FPGA banks, to the minipods as well as to all other card's components.

- Clocking circuitry that provides low-jitter clock to the transceiver banks of the FPGA. The circuitry includes clock generators, jitter cleaner and cross point switches in order to feed all GTH transceivers with a reference clock (refclk). The clock source depends on the MP7 configuration and can be either an on board oscillator or the "LHC" clock provided to the backplane.

- An ultra-fine-pitch connector with 30 differential pairs to/from the FPGA with which the processor is able to send LVTTL signals to the TCDS system and LDVS signals to the legacy Global Trigger in order to be used as external condition.

The cooling of the FPGA is achieved with a large heat-sink and the μTCA crate's fans. The provided power on each AMC slot of the crate is sufficient for the power consumption of the MP7. The FPGA of the MP7 acts as the master of the card and controls all its devices. The FPGA is accessed by ethernet connection using one of its transceivers. The architecture of the *XC7VX690TFFG1927-2* FPGA provides 20 transceiver quads from which the 2 uppermost together with the corresponding blocks of logic (co-called banks) instantiate the readout and the infrastructure logic of the system. The other 18 quads provide the 72 full-duplex 10 Gb/s data transmission links and the remaining 70% of the FPGA (18 banks) provides the necessary resources to implement the BMTF algorithm [31].

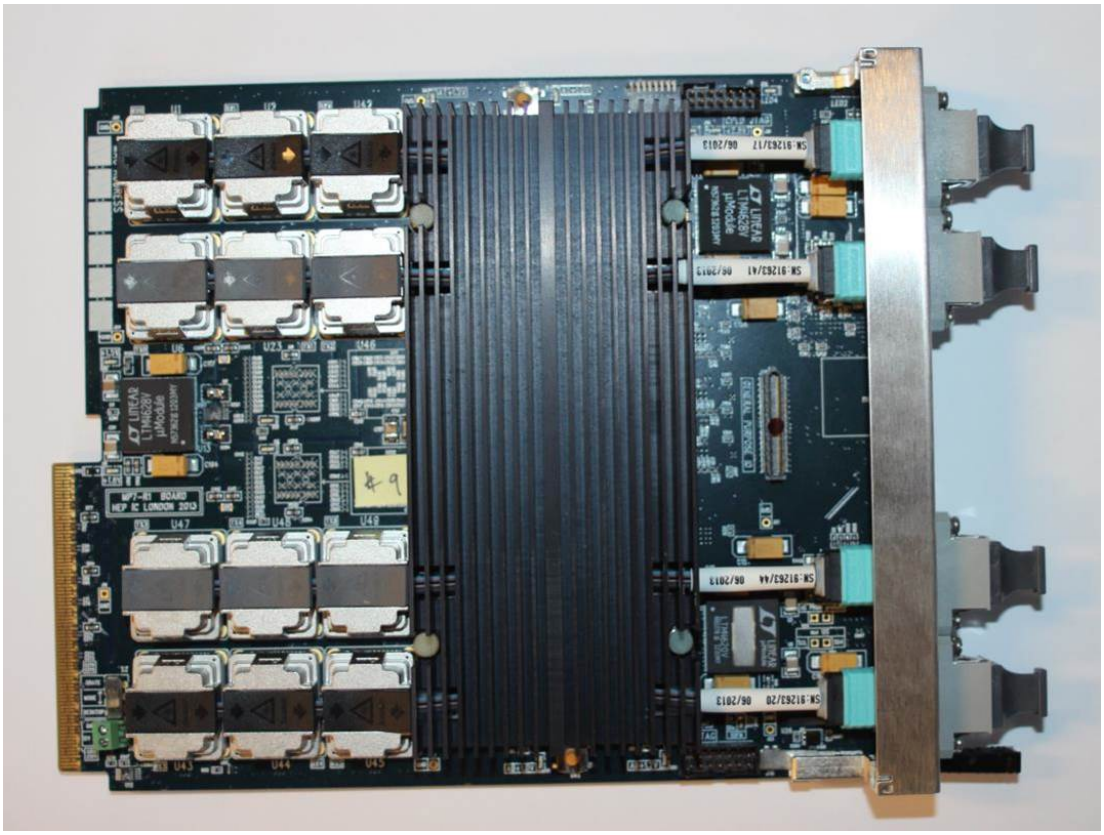


Figure 4.15: The XE type MP7 card is used in the BMTF system. 12 minipod optics (showing on the left side next to the heat exchanger) are connected via multimode fiber to 4 MTP connectors (front panel).

4.4 BMTF implementation

The BMTF firmware follows a common set of logic blocks used in all trigger systems that use the MP7 hardware [57]. This framework contains logic blocks presented in Figure 4.16. The block diagram contains the BMTF ALGO, the readout

(DAQ) block, the TTC block and the general infrastructure. The BMTF ALGO corresponds to the track finders that are used to trigger muons candidates. The MP7 set of logic blocks instantiates all the needed interfaces and control the logic of the system.

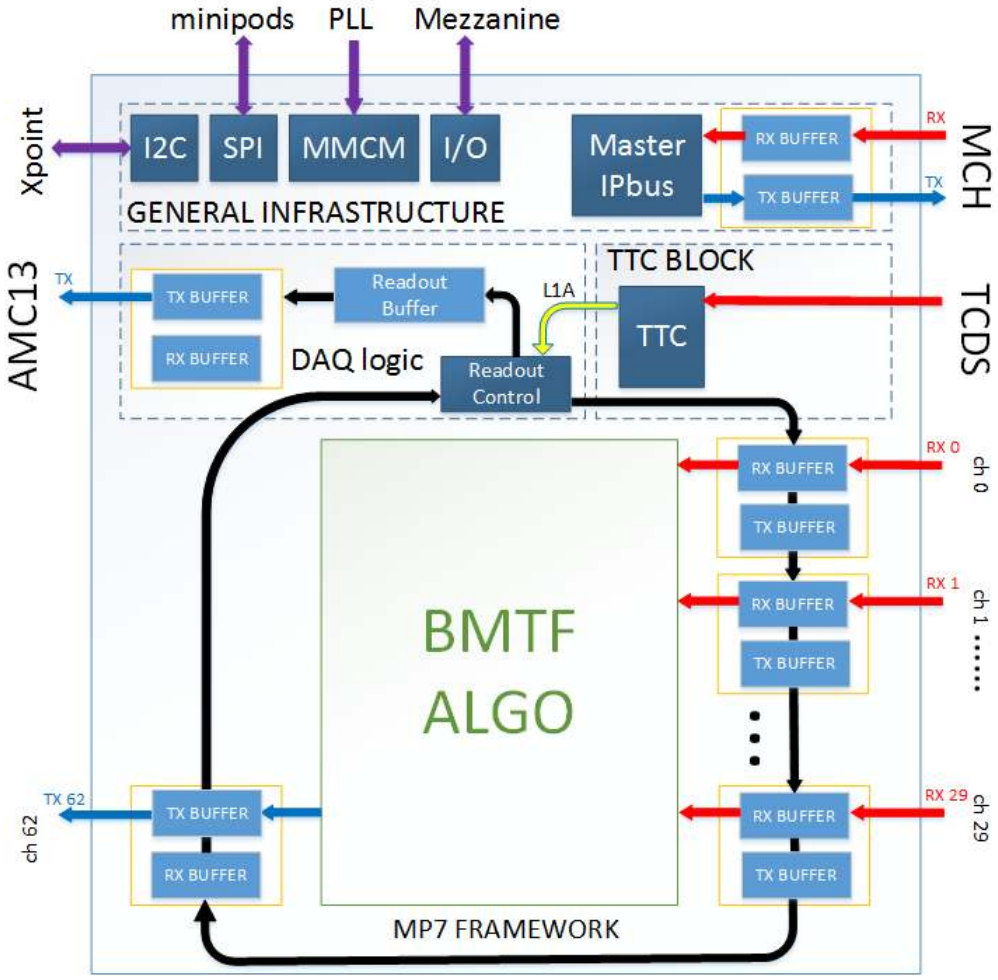


Figure 4.16: Block diagram of the BMTF firmware. The core of the logic is the BMTF algorithm and wrapped around the set of logic blocks (framework) that supports the core and implement all needed functions: serializes/deserializes, DAQ and TCDS interface, control of the system through ethernet (IPbus) and control of on-board components.

Shown of the left top of Figure 4.16, the general infrastructure which instantiates an I^2C interface to control a Xpoint switch which distributes the low jitter clock to the transceivers of the FPGA, a SPI interface to enable the optics of the card (minipods) and read their receiving light power, an I/O array of three state buffers to export technical trigger signals to a mezzanine card and an IPbus block that implements an IP-UDP interface between the FPGA and the control PC and provides the needed infrastructure to control and monitor the design.

The TTC block receives Timing Trigger Control (TTC) comands like resynchronization, reset and control commands (BGo) from the Trigger Control and Distribution System (TCDS) [58]. The TTC block delivers the L1A signal to the readout block of the design. It also reads the status of the DAQ block and

applies bandwidth throttling when is needed. Finally, it reconstructs the LHC clock from the serial datastream of the TCDS, procedure that is crucial to keep the design synchronous with the rest level-1 trigger system.

The DAQ block collects all input and output data of the BMTF processor every time it gets the L1A signal from the TTC block. It uses a ring architecture with a daisy chain bus that interconnects the channel buffers with the readout buffer and tags the data according to corresponding channel and data direction (RX-TX) (Figure 4.17). The readout logic adds a header and a trailer to the data and sends the data packet to the AMC13, which finally forward the packets to the Front-End Driver (FED) with 10.3 Gb/s bandwidth.

The MP7 set of logic blocks includes also the implementation of up to 72 serial links and supports the asynchronous 10-Gb/s protocol which is described in the Subsection 4.4.1.1. The set of logic blocks contains also two buffers for each channel, one per data direction (RX and TX BUF) and 1024 words long that are used with multiple configurations. The buffers as well as the configuration logic are shown in the Figure 4.17.

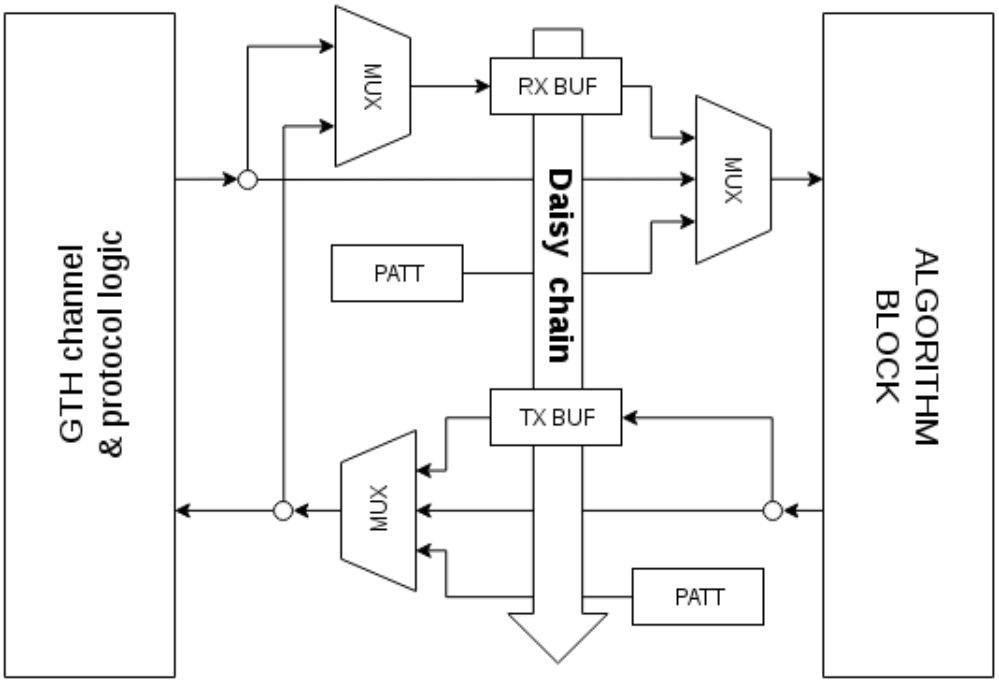


Figure 4.17: Block diagram of MP7 buffers and their configuration logic: The buffers (RX BUF, TX BUF) are 1024 long and 32-bits width. A set of multiplexers is controlled by the configuration and set the buffers in normal, test or DAQ mode. In normal mode the buffers capture data which pass though. In test mode the buffer are used to send data to the algorithm or to the optical links. In DAQ mode the buffers are connected in a daisy chain data flow and collect data to be sent through the DAQ.

The MP7 buffer circuitry is used in normal operation as well as for testing. As shown in the upper side of the block diagram the algorithm block receives data from three different sources which are determined by a multiplexer. First, during normal operation, it receives data from the input stream, secondly it can get test patterns from a pattern generator (PATT) and thirdly it can get data from the RX buffer

that have been injected through IPbus. The third option is used in the evaluation of the algorithm with muon patterns. The RX buffer also can receive data from the output stream (lower part of the diagram) which applies a data loopback. In the TX side, data are sent from three sources as in the RX side: from a pattern generator machine, from the algorithm output (normal operation) and from the TX buffer. As it happens in the RX side, data can be injected to the TX buffer as well and sent to the GTH transceivers. In collision or cosmics run at CMS, both RX and TX buffets are collecting data from the data stream and are accessed by a daisy chain configuration in order to send the data to the DAQ block of the MP7 framwork.

The buffer circuitry has been wildly used in the evaluation of the BMTF algorithm, in the installation and in the commissioning of system at USC55 cavern of CMS.

4.4.1 Serial I/Os

TwinMux applies three different link protocols using the GTH transceivers: To receive data from DT minicrates, it uses the synchronous protocol at 480 Mb/s with which it receives 12-bits every 25 ns. To receive RPC links the TwinMux uses the CERN designed GOL protocol which runs at 1.6 Gb/s. This protocol uses 8b10b decoding which corresponds to a payload of 1.28 Gb/s and 32 bit at 40 MHz. In order to avoid link errors because of LHC clock phase uncertainties, the system applies a data-over-sample technique. In the transmitting side the asynchronous 9.6-Gb/s protocol is used. The logic for this protocol is common in all L1 Trigger subsystems and is briefly described in the next subsection.

The BMTF uses the same asynchronous 9.6-Gb/s link protocol as well to receive data from TwinMux and avoid errors due to instabilities in the LHC clock. Also in the transmitting side BMTF uses the same protocol.

4.4.1.1 Asynchronous Protocol

This protocol is designed based on 10 Gb/s serial links with 8b/10b encoding [59] which gives a usable bandwidth of 8 Gb/s and a payload of 32 bits at 250 MHz (Appendix F).

Frames numbers	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	
240MHz domain (ns)	4	8	13	17	21	25	29	33	38	42	46	50	
250MHz domain (ns)	4	8	12	16	20	24	28	32	36	40	44	48	
Frames numbers	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**	**25**
240MHz domain (ns)	54	58	63	67	71	75	79	83	88	92	96	100	
250MHz domain (ns)	52	56	60	64	68	72	76	80	84	88	92	96	100

Table 4.3: Time stabs of the two-clock domains in the Asynchonus serial protocol: 250 MHz is the Transceiver clock and 240 MHz the algorithm clock. The last frame of the 250-MHz clock domain is filled with a comma.

The asynchronous protocol used in the TwinMux - BMTF interconnections as well as in the BMTF - μGMT, is based on the above commercial protocol with one additional comma word injected every 25 frames in the 250-MHz clock domain. This additional frame merges the two different bandwidths (10 Gb/s and 9.6 Gb/s) and ensures that the unstable LHC clock does not affect the serial link stability. This mechanism occurs in the crossing of the two domains between the transceiver user

clock (250 MHz) [60] and the algorithm domain clock (240 MHz). The algorithm clock is slower than the user clock and both are running in 32-bit buses. As it is shown in Table 4.3, the time stabs of both domains get the same value (100.0 ns) after receiving 25 frames of 250 MHz and 24 frames of 240 MHz. On the transmitter side, the asynchronous protocol adds the extra comma frame in the 250-MHz domain. In the receiver, the protocol uses the comma to find and correct any phase change between the two-clock domains. The asynchronous 32-bit bus runs at 240 MHz giving the payload 7.68 Gb/s and the total bandwidth is 9.6 Gb/s. The link protocol checks the transmission of the data with a CRC check sum that is calculated over an LHC orbit. This procedure is executed when TCDS suppresses all triggers in the orbit gap. After locking the links, the BMTF deserializers convert the pairs of 32-bit input channels to a sequence of 384 bits and run the BMTF algorithm at 160 MHz.

4.4.2 BMTF Latency

Reducing the latency is one of the most important aspects in the level-1 trigger upgrade. This Section describes the latency improvement as well as the latency cost for each one of the logic blocks of the BMTF algorithm before and after the upgrade.

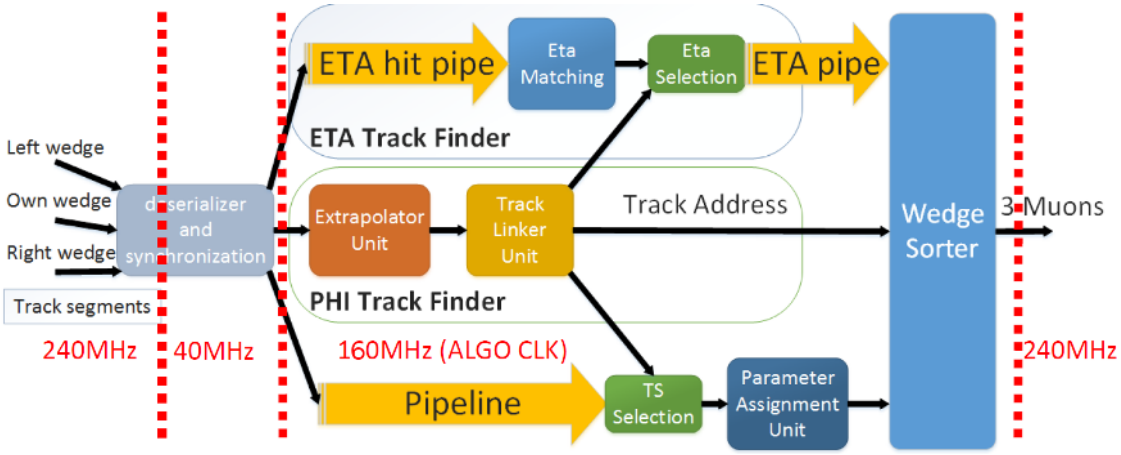


Figure 4.18: The BMTF algorithm blocks, divided in three different clock domains: The 240-MHz domain where the 10-Gb/s links are implemented, the 40-MHz domain where the input data are formatted and concentrated and formed and the 160 MHz where the BMTF algorithm is running.

As explained in the previous section the BMTF algorithm is divided in logic blocks. The BMTF algorithm is faster than the old DTTF despite the fact that their main architecture for both legacy and upgraded algorithm is almost the same, as they use similar algorithm blocks, but they differ in the operation frequencies. The DTTF algorithm was running with 40-MHz clock while the BMTF takes advantage of the bigger logic capacity and the higher frequency clocks that the Virtex-7 FPGA provides for the algorithm (Figure 4.18). BMTF both in receiver and the transmitter uses 20 at 240-MHz clock cycles (20 x 4.16 ns). The deserializer & synchronization block run in 1 at 40-MHz clock cycle (1 x 25 ns) and the algorithm core runs in 14 at 160-MHz clock cycles (14 x 6.25 ns). The bunch crossings with the corresponding clock domains for all algorithm blocks used in the old (DTTF) and the upgraded (BMTF) design are presented in the Table 4.4.

	DTTF			BMTF		
Algorithm part	**bx**	**Clock domain**	**Cumulative bx**	**bx**	**Clock domain**	**Cumulative bx**
Input	-	-	0	1 + 2/6	240MHz	1 + 2/6
Synchronization	3	40MHz	3	1	40MHz	1 + 2/6
Extrapolation	2	40MHz	5	2/4	160MHz	2 + 5/6
Quality Sorter	2	40MHz	7	unused	-	2 + 5/6
Track Assembler	9	40MHz	16	2+1/4	160MHz	5 + 0.5/6
Param. Assign.	2	40MHz	18	parallel	160MHz	5 + 0.5/6
Wedge Sorter	2	40MHz	**20**	3/4	160MHz	**5 + 5/6**

Table 4.4: Latency budget of the barrel track finder algorithm before (DTTF) and after (BMTF) the trigger upgrade.

The total latency of the BMTF algorithm has been significantly reduced from 20 bunch crossings, DTTF to $5 + \frac{5}{6}$ bunch crossings. The saved 14 BXs + $\frac{1}{6}$ are used by other subsystems of the trigger chain (like TwinMux) in order to give the needed time to generate the super-primitives as described in the Section 3.1.2. Finally, the BMTF design compared to the DTTF has been optimized developing a more parallel architecture. This was realized thanks to the large FPGA of the MP7 card used in the BMTF.

	DTTF		BMTF	
Stage	**bx**	**Cumulative BXs**	**bx**	**Cumulative BXs**
RX block	5	5	2	2
Sync with CSC	1	6	not used	2
Algorithm	20	26	5 + 5/6	7 + 5/6
Global Muon Sorter	4	30	Moved to μGMT	7 + 5/6
TX block	1	31	2 + 3/6	10 + 2/6
Cable to GMT	2	**33**	2 + 4/6	**13**

Table 4.5: Total latency of the BMTF and DTTF. Measured from the input receiver of the BMTF to the input receiver of the μGMT.

Furthermore the latency in the new system of the logic that receives and transmits the data to the input and from the output of the algorithm has been reduced. Table 4.5 shows that the receiver block of the DTTF needs 6 bunch crossings but the same block of BMTF only 1. In addition DTTF needs 26 bunch crossings to sort the output of the algorithm and send it to the μGMT input while BMTF needs $7 + \frac{5}{6}$ (the muon sorting has been moved to the μGMT).

As can be deduced from the above, BMTF is almost three times faster than the old DTTF. Considering that in the upgraded system the Global Moun Sorter algorithm part is running in the μGMT, the BMTF needs totally **13 bunch crossings** to deserialize the input data stream, to find the best 3 muon tracks within one wedge of the barrel area of CMS, to assign their parameters (p_T, ϕ, η, quality bits and track addresses), serialize the output and send the results to the micro Global Muon Trigger.

4.4.3 Firmware optimization

The first version of the BMTF firmware was running using the 40-MHz clock. The firmware was optimized to run using 160-MHz frequency clock. The wedge sorter block has been rewritten from scratch (Appendix E, Section E.3) fact which trimmed timing issue in the implementation. After solving all timing issues the design was able to run at 160-MHz clock and the latency of the algorithm is reduced from 20 bunch crossings to 5. Moreover the logic of the FPGA was divided to blocks which help design constrains to be applied. In Figure 4.19, the yellow block has the input transceiver quads with the additional logic to implement the alignment procedure, the cross domain to implement the asynchronous protocol and the RX channel buffers to capture or inject data. The green block is one additional quad that contains the same logic as the input, but is used as output. The red block has all the algorithm logic. The light blue the readout logic that implements a daisy chain bus, a readout buffer and the logic to make packets to be sent to the DAQ when a L1A arrives.

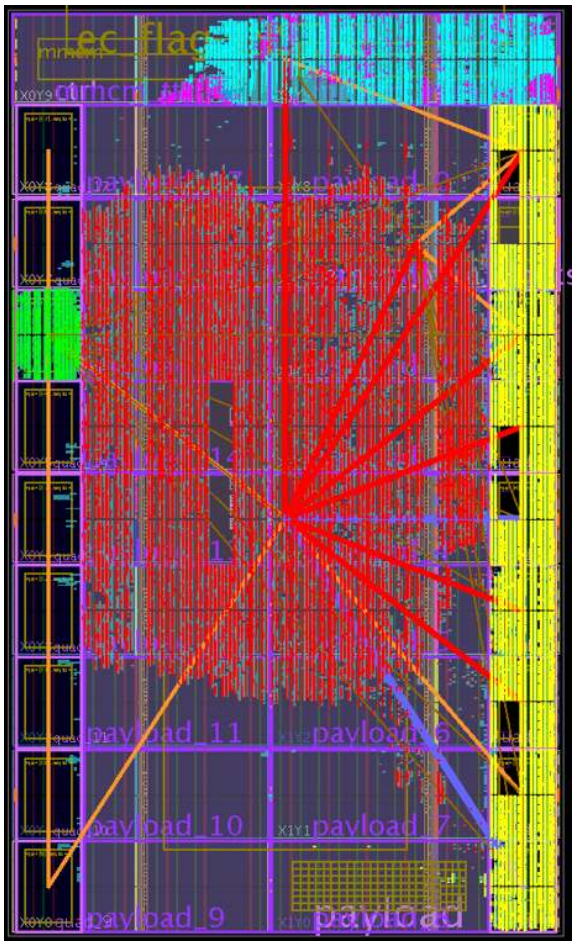


Figure 4.19: Implementation of the BMTF in the FPGA die.

Resource	Utilization	Available	Utilization %
LUT	142155	433200	32.8
LUTRAM	12453	174200	7.1
FF	102268	866400	11.8
BRAM	501	1470	34.1
IO	129	600	21.5
GT	42	80	52.5
BUFG	8	32	25.0
MMCM	3	20	15.0

Table 4.6: Post implementation report of the FPGA used resources

The purple block is the top level of the logic and contains the general infrastructure of the system (IPbus, SPI, MMCMs, I/O and control logic). In the final version of the BMTF, the unused quads are not instantiated fact that saves power and resources consumption. As shown in Table 4.6, approximately $\frac{1}{3}$ of the FPGA resources are used, a fact that allows for future expansion.

4.4.4 Latency improvements

After installation and during commissioning, the latency of BMTF changed several times in order to reduce the processing time and deliver muon candidates to μGMT on time. Moreover, the latency reduction, has increased the available processing time for potential future BMTF algorithm improvements as well as for improvements in the TwinMux or μGMT systems.

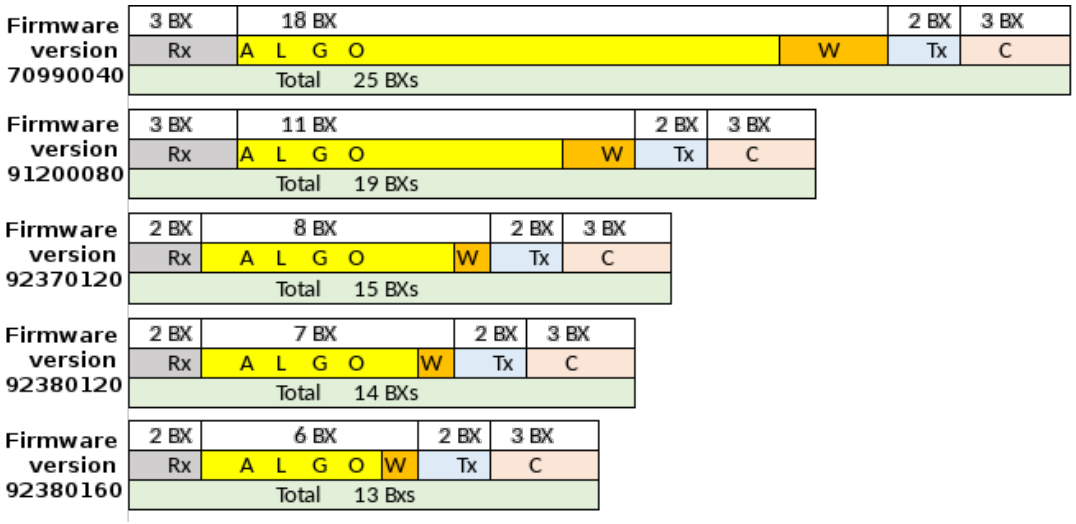


Figure 4.20: The latency of five BMTF firmware versions. Bx: Bunch crossing time (25 ns). Rx: Receiver (deserializer) block, ALGO: Algorithm block, W: Wedge sorter block, Tx: Transmitter (serializer) block, C: delay due to cable length from the output of BMTF to the input of μGMT. The last three digits of the firmware version indicate the clock frequency in MHz used in the BMTF algorithm.

The BMTF firmware controls the Phase-Locked Loop (PLL) circuit and can generate frequencies (multiples of 40 MHz) used in the algorithm block. Higher clock frequency reduces the processing time of the algorithm but, eventually generates timing errors. A timing error is issued when a signal needs more time to travel from a source flip-flop to a destination flip-flop than a limit, set by the clock of the flip-flops. The required time is defined by the period of the clock. For instance a 80-MHz clock has 12.5 ns period available processing time. Figure 4.20 shows the latency given in bunch crossings (BX) for five firmware versions. The last three digits of the firmware version indicate the clock frequency in MHz used in the BMTF algorithm. The first upgrade (80 MHz) didn't introduce timing errors. The second upgrade (120 MHz) required a slightly different architecture. Parts of the design, like the wedge-sorter block, were rewritten from scratch and flip-flops were replaced. The third upgrade uses the same clock as in the previous but the logic was farther optimized by removing a few unnecessary latches. Finally, the last upgrade provided timing errors between the output of the algorithm and the input of the serializer block. The algorithm's clock domain uses 160 MHz instead of 120 MHz and serializer's domain uses 240 MHz.

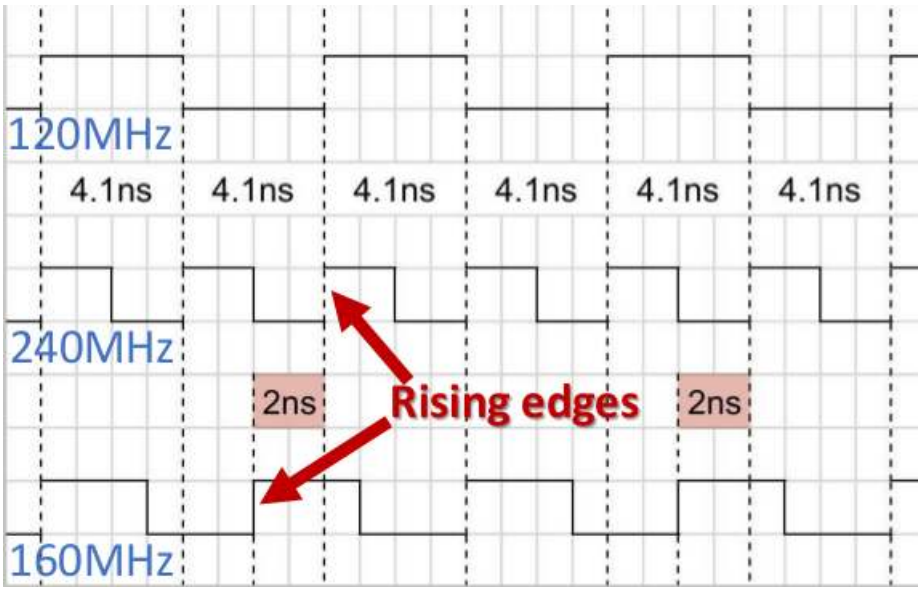


Figure 4.21: Phase difference between clock domains

All clocks in BMTF are generated using the same PLL and thus having known phase differences. In firmware version *92380120* data are safely crossing from 120-MHz to 240-MHz clock domains because the minimum required time for the signals to cross these domains is a period of the 240-MHz clock (4.167 ns). But as shown in Figure 4.21, when the data must cross from 160-MHz to 240-MHz clock domains, the minimum required time is half of the 240-MHz clock period (2.083 ns) and the serializer is not designed to meet this requirement.

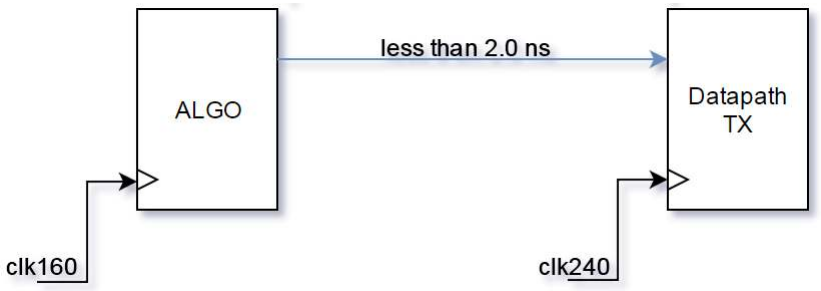


Figure 4.22: 160-MHz to 240-MHz bridge. Constrain force implementation tool to place the flip-flops close to each other.

In order to reduce the time delay between 160-MHz and 240-MHz clock domains, a constraint was applied. In the last firmware version a timing constraint is used to force the flips-flops of the 160 MHz - 240 MHz in the bridge (Figure 4.22) to be placed in space close enough in order to make 2.0 ns a sufficient time for the signals to cross the flip-flops.

4.5 Future improvements

This section presents some ideas of further improvements of the BMTF without introducing any change in the algorithm architecture. Those suggestions are listed below and grouped in certain tasks:

1. **VHDL structure**: Some parts of the code have been taken from the old DTTF system and have been reused in the BMTF. Many blocks of such code have been rewritten in order to get full advantage of Virtex-7 resources but there are blocks that they are not optimal for 7-series Xilinx FPGAs. Improving the structure will give the possibility to spot small code bugs that have never been observed before and to increase the algorithms clock from 160 MHz to 240 MHz. The latter should reduce the latency at least by one bunch-crossing time.

2. **Latency reduction**: The synchronization block (Figure 4.18) is running at 40-MHz clock domain. Modifying this block will reduce the latency by 5/6 of a bunch crossing.

3. **System architecture**: The BMTF trigger could be running on 6 instead of 12 MP7s. In this case each card will run the algorithm for two wedges instead of one. This is possible because the resources used to run the algorithm in the current FPGA do not exceed the 1/3 of the available. The used links are 30 out of 72 available. With this change, the system will be duplicated and a second identical system will be available to replace the main, in case it fails.

4. **System redundancy**: As described in the end of Section 4.2, after suppressing the data of bunch crossings 2, 1, -1 and -2, the BMTF splitting into two crates is no longer needed. That's because one DAQ optical link can serve the whole system. Putting 6 MP7s in one crate will leave the second with the other 6 MP7s as a fallback crate ready to operate. The second crate can replace the main one in case of any type of malfunction. This action requires "VHDL structure" task to be completed first. The fallback crate will be ready to run the BMTF system after a simple intervention where the MTP trunk cables of the main crate will be disconnected from the main crate and connected to the fallback crate.

5. **System reliability**: The most reliable system is the one that never needs to reboot. As will be described in Section 5.3, during BMTF commissioning, corrupt data were observed. The cause was a random phase shift of the system clock (also called LHC clock) that happens when CMS running mode is switched from cosmics to collisions. The FPGA memories of Virtex-7 are not made to tolerate this clock distortion and the stored data can get corrupted. As a workaround to this problem, the memories are reloaded each time CMS starts a new run. Since Read Only Memories (ROM) are implemented in the BMTF firmware, the whole firmware is reloaded to the MP7s and the system is starts over on every run. Hence, the uptime of the BMTF is short and this prevents a continuous monitoring. To address this issue, instead of ROM memories, Random Access Memories (RAM) can be implemented in the BMTF firmware. This change will give the possibility to rewrite the BMTF memories instead

of uploading the firmware which starts the system from scratch and resets its uptime. The most straightforward way to implement such memories on MP7 "like" firmware is to add a bridge logic with IPbus interface to RAM memories and upload data from the CMS database on each CMS startup.

6. **Utilization reduction**: This VHDL design still contains memories which were used initially for testing proposes. Since BMTF algorithm is integrated with MP7 design, those memories are unnecessary and can be removed. Also task 1 can potentially decrease the FPGA utilization.

7. **p_T dynamic range**: As presented in Appendix C, the p_T is expressed by 9-bits and a 0.5 GeV precision. Table C.1 shows that in the output of the system there are unused bits (NC). Two of these bits could increase the p_T word from 9 to 11-bits. This would increase the dynamic range from 512 to 2048 with a new step of 125 MeV, resulting in the increase of the required space for the corresponding LUTs. The Virtex-7 FPGA used in the BMTF has the extra memory to support the larger LUTs. The output-bit allocation can remain as is. p_T bits 0 to 8 of 0, 2 and 4 words can be used for the most significant 9 bits of the new p_T and bits 2 to 3 of 1, 3 and 5 words can be used for the least significant 2 bits. No change is needed in the readout part except from unpacking. This upgrade does not necessarily require any change in the μGMT trigger because the dynamic range of the 9 most significant bits gives the current dynamic range.

8. **Easier maintenance**: To maintain a VHDL design it helps to make it more parametrizable and use "generates" in code can be an good option. This will reduce the total number of code lines and will make the design easier to be understood and more configurable.

9. **Commissioning of a new algorithm**: Since only 1/3 of the FPGA resources are used, the user can implement a second algorithm in the same FPGA and run it in parallel with the BMTF algorithm. While the BMTF runs normally in CMS, the new algorithm can run off-line. Then one additional DAQ channel can be used with the new algorithm in order to send L1A triggered events to the DAQ. In addition, the system can be build flexible enough to switch the trigger decision from the BMTF to the new algorithm. On this way efficiency and trigger rate can be compared between the two algorithms.

All above tasks require task 1 to be completed first.

Chapter 5

Validation and Commissioning of the BMTF system

The upgraded BMTF has been exhaustively tested in the laboratory before being installed in the CMS USC55 cavern. After the installation, great effort took place underground to commission the system and solve many problems that occur in the hardware, software and firmware. The BMTF was fully operational before LHC started colliding proton bunches in 2016 and the magnet of CMS reached the nominal magnitude of 4 Tesla. BMTF hardware output agrees with the results taken from a software emulator of the BMTF at the level of 98%.

5.1 Validation of a BMTF slice in the Laboratory

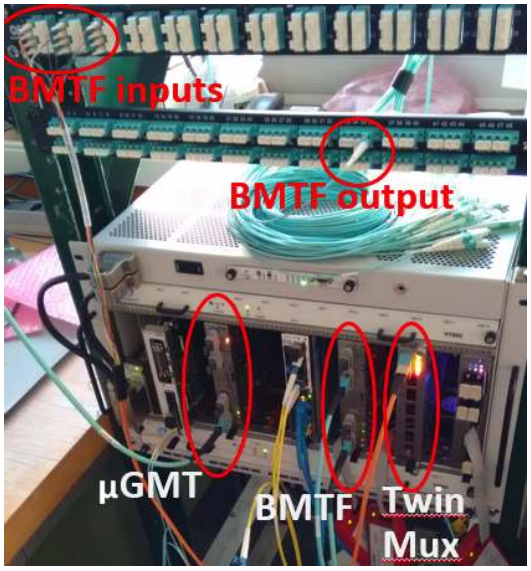


Figure 5.1: BMTF test-stand

As described in Chapter 4, each BMTF processor searches for muon tracks within a wedge of CMS and therefor all processors run the same algorithm, implemented in a MP7 board. As mentioned in the same Chapter every BMTF card receives data primitives from the TwinMux system and sends the results to the μGMT system which is implemented in a second MP7 card. BMTF system is modular. Only one slice of BMTF algorithm can validate its good performance. As described in 4.1.2, slice of algorithm is the PHI Track Finder (PHTF). The PHTF was tested in the laboratory with primitive patterns. Figure 5.1 shows the setup of the validation test. A TwinMux is used to send all twelve inputs to PHTF; one MP7 runs the BMTF firmware and a second MP7 is used to replace μGMT, capture the data and send them for analysis. On the top of the Figure two patch panels are shown. The upper connects the twelve output fibers of the TwinMux with equal number of BMTF input fibers and the lower connects the output fiber of BMTF with the input fiber

of μGMT. All cards are synchronized and receive TTC commands from the AMC13 card which also provides a common clock.

5.1.1 Algorithm validation with injected muon patterns

The PHTF was tested using artificial muon candidates. Raw data with single muons were generated using the CMS Monte Carlo simulation software. This Monte Carlo data was injected to the output buffers of the TwinMux hardware. The TwinMux sent the muon patterns to the BMTF and the results are sent to the μGMT-MP7. Finally, software was used to read the input buffers of the μGMT and the results were compared with the results from a bit-to-bit emulation of the BMTF. Statistical samples from Monte Carlo events are used to check for eventual discrepancies and to show the performance of the algorithm.

Figure 5.2 shows the normalized difference of the muon parameter coming from the hardware output minus the output of the emulator p_T, ϕ and in *quality bits*. 20,000 muon candidates, are used generated with flat p_T range, from 6 GeV up to 1 TeV.

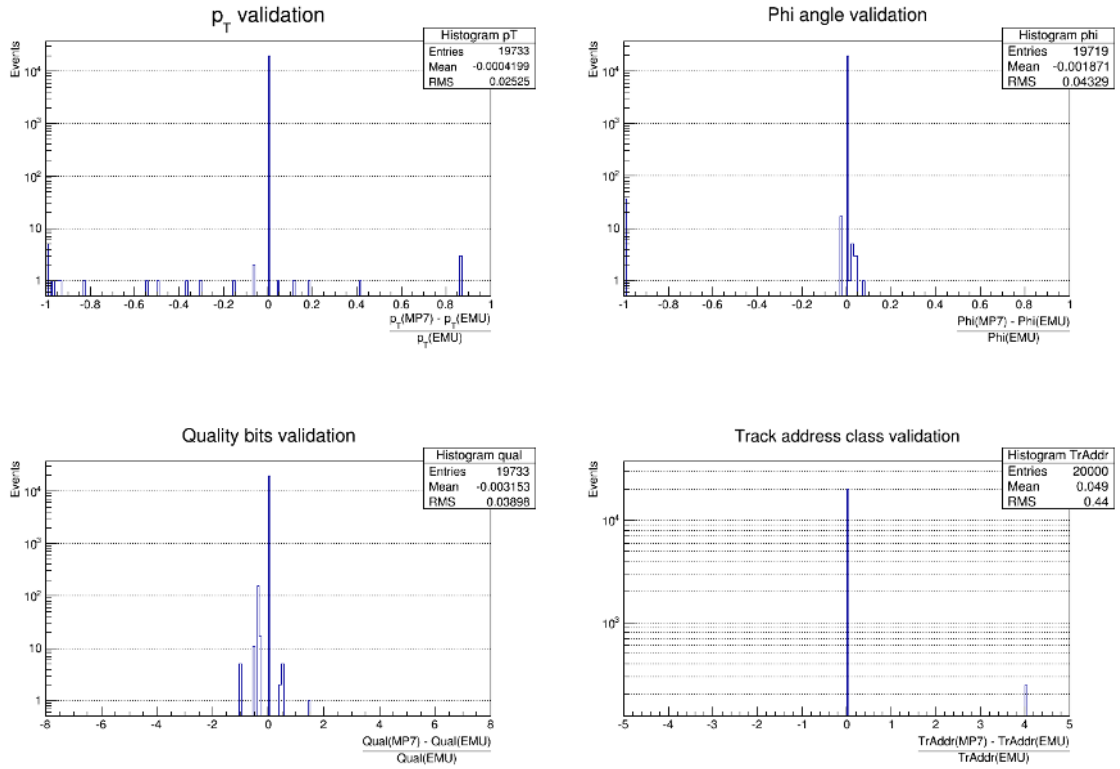


Figure 5.2: Histograms of hardware algorithm output compared with emulator output (p_T, ϕ, quality bits and track addresses). Magnitude: $\frac{X_{MP7}-X_{EMU}}{X_{EMU}}$, where X: p_T, ϕ, *Quality bits*, *Track Address*

39 LUT discrepancies found in p_T, 68 in ϕ, 196 in quality bit and 245 in the track addresses out of 20,000 events. The result proves that the hardware and the emulator are in good agreement and the algorithm of the old DTTF algorithm has been successfully implemented to the new BMTF framework [2].

The plot in the left-hand-side of Figure 5.3 shows that the p_T difference as a function of emulator p_T is mostly stable at zero, except of a few points, demonstrating the very good agreement between the emulator and the MP7 firmware. The right-hand-side of Figure 5.3 shows that the ϕ difference as a function of emulator ϕ is mostly stable at zero, except very few cases most of which have small ϕ difference. The small number of discrepancies shown in both plots were fixed after installation stage (Subsections 5.4.1 and 5.4.2).

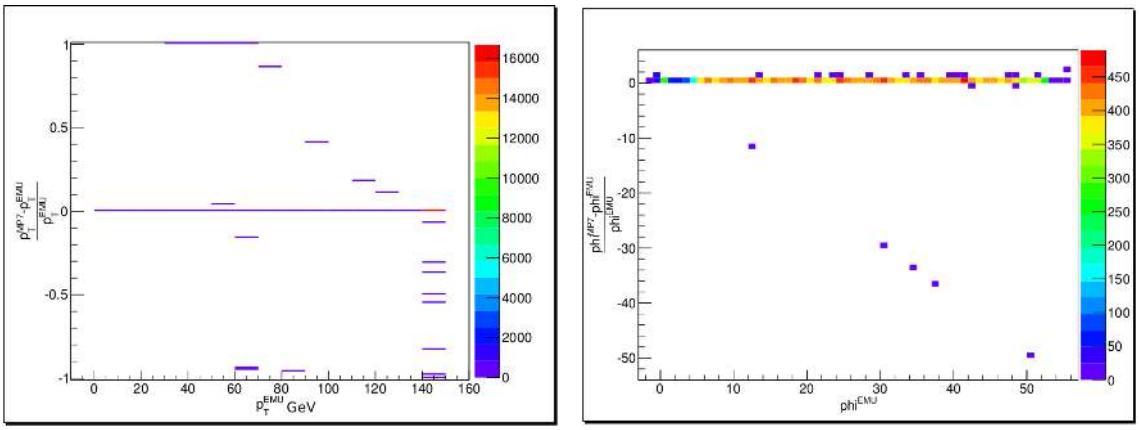


Figure 5.3: Hardware resolution, versus emulator p_T and ϕ histograms.

5.2 Validation of a BMTF slice in USC55 cavern

During the last quarter of 2015 a part (slice) of the BMTF trigger was installed (rack S1D03) in USC55 cavern at CMS. Figure 5.4 shows the BMTF processor and the patch panel connecting the output links of 6 TwinMuxs with the input links of the BMTF processor. The processor was receiving data from the sectors 9, 10, 11 of the wheels -2, -1. The results of the BMTF were successfully sent to the μGMT.

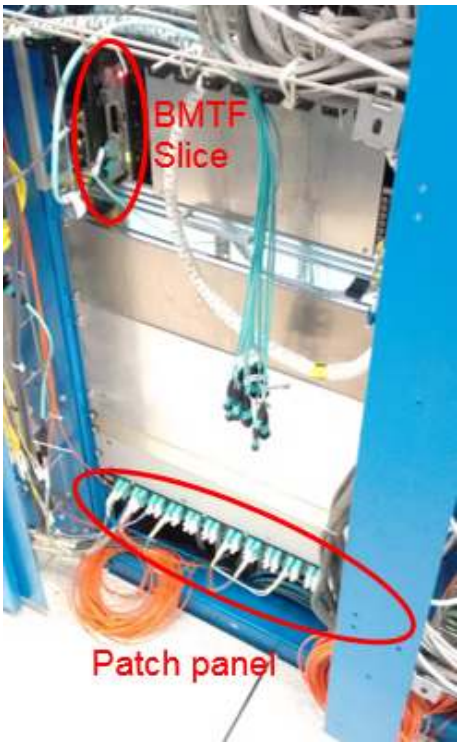


Figure 5.4: BMTF slice in USC55

The BMTF slice was running in parallel with the DTTF in order to compare the trigger rate of the two systems. The trigger rate of the BMTF was extracted form the MP7 to a Low Voltage Differential Signal (LVDS) via a mezzanine card. The signal was connected to the old Global Trigger (GT) which was generating a technical trigger each time the BMTF slice found a muon. On one hand the technical trigger bit 22 was observed in the online monitor of the Global Trigger (Figure 5.5) and on the other hand the equivalent PHI Track Finders (PHTFs) of the DTTF system were recorded via the Data Quality Monitoring software (Figure 5.6).

The plot of the technical bit referring to the BMTF slice, was compared with the sum of the trigger rates of the corresponding PHTFs. The sum was driven by the fact that in the upgraded system, one BMTF card hosts six PHTF blocks and in this slice test the BMTF was connected only to wheels N1 and N2 of sector 10.

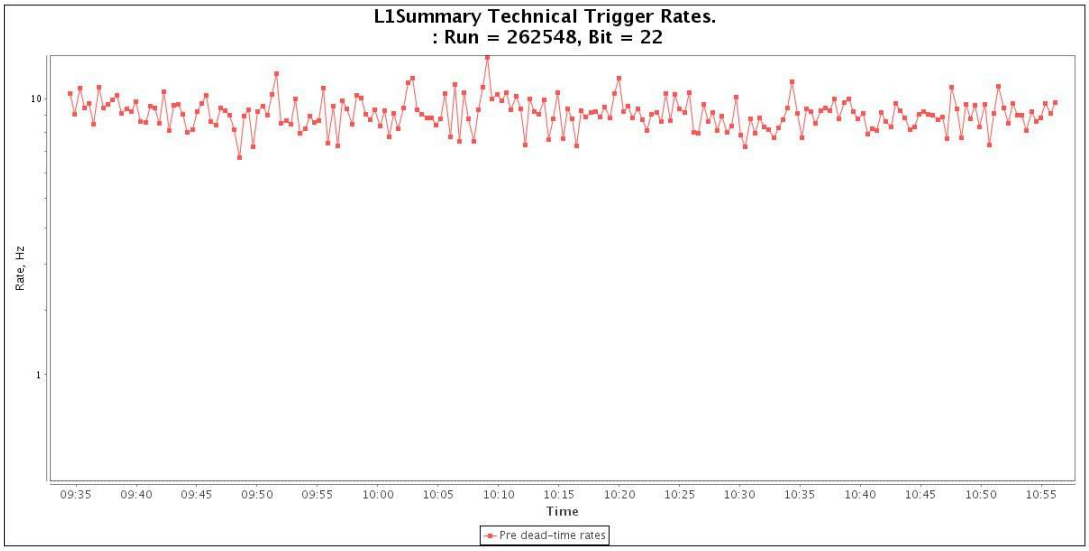


Figure 5.5: BMTF-slice trigger rate during the CMS run 262548

The plot of the technical bit (Figure 5.5) used to monitor the rate of the BMTF slice under the CMS cosmics run 262548. As it is shown in the vertical axis, the mean rate is about 10 Hz. Figure 5.6 shows the trigger rate of the -2, -1, -0 PHTFs of the DTTF. The mean value of the trigger rate of -2 wheel (blue color) PHTF is about 6 Hz and of one of -1 wheel (green color) PHTF is about 5 Hz. The sum of the -2 and -1 PHTF is approximately 11 Hz which is a little higher than the BMTF rate.

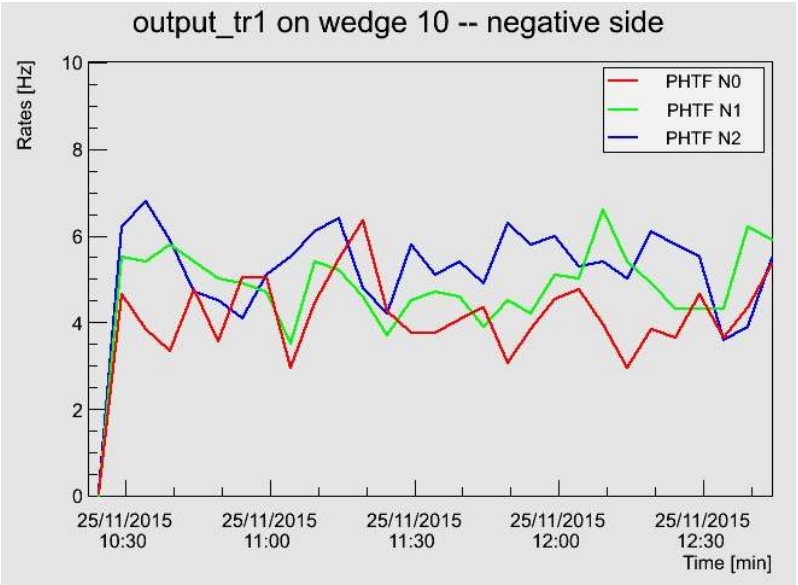


Figure 5.6: DTTF trigger rates of sector 10, positive wheels, PHTFs during the CMS run 262548

The 1 Hz trigger rate difference is reasonable because, unlike BMTF, the DTTF was receiving data also from the endcaps of the CMS (CSC data), a fact which under cosmics rays, slightly increases the muon rate. This test proved that BMTF was triggering with an expected rate and was ready to be integrated with Level 1 Trigger system and tested farther on commissioning stage.

5.3 Installation and Commissioning of the system

On January of 2016 the old sector collector (SC) in CMS was replaced by the TwinMux system. DTTF was no longer receiving inputs from the SC and therefor stopped working. One additional crate and all the twelve processors were installed to BMTF in order to be fully operational. In total, 360 optical links were connected to the TwinMux output patch panel in order to establish the TwinMux - BMTF data transmissions [6]. Moreover, 12 optical cables used for the BMTF to μGMT connections [61]. In the rear side of BMTF crate (5.9 middle) a power supply was installed to feed 8 power modules (4 to the upper and 4 to the bottom) for both BMTF crates.

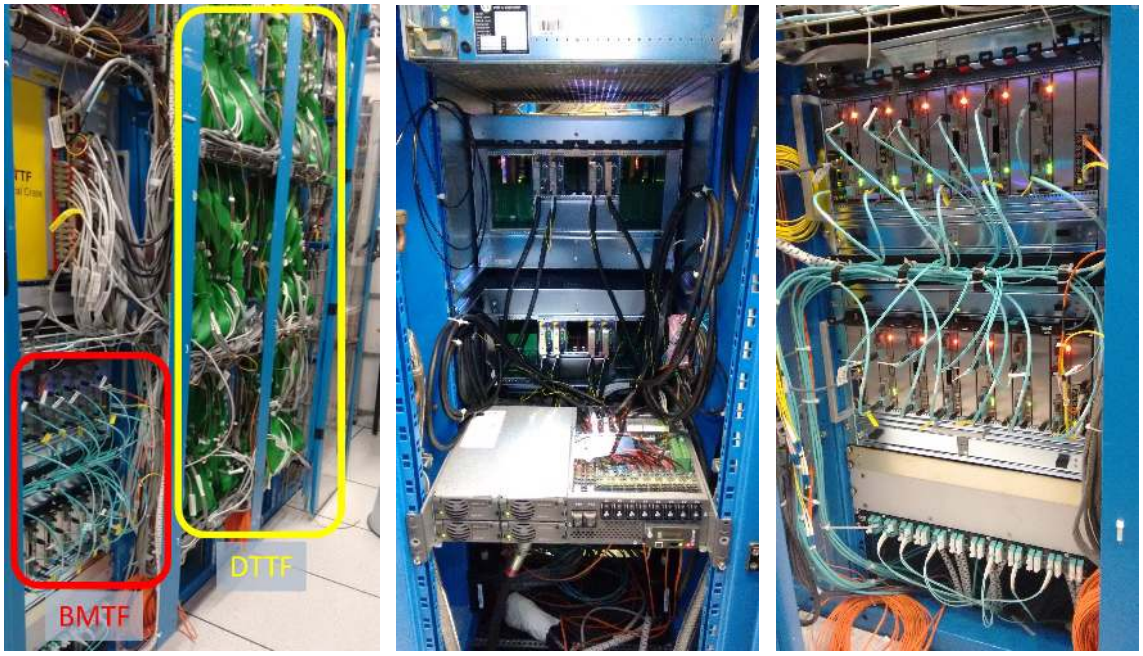


Figure 5.7: The BMTF system installed in CMS. Left: BMTF and DTTF systems. Middle: Rear side of BMTF crates. Right: Front side of BMTF crates.

Figure 5.9 left, shows both DTTF and BMTF configurations in the USC55 cavern and Figure 5.9 right, the view of BMTF after the installation was completed. During commissioning few communication problems were found in the 372 optical links. Faulty minipod optics broken cable were fixed.

Figure 5.8 shows the histogram of p_T values for every wedge processor taken from BMTF during the commissioning. The fifth and the twelfth card were giving p_T values lower than 3 GeV. Those values were not expected since as explained in Section 4.1.2.3, the physical values in the output of the BMTF algorithm are assigned by LUTs (memory components called BRAMs) and the lower values written in those LUTs is 3 GeV. The firmware to emulator comparisons (Figure 5.9 left side) shows the impact of this symptom in the p_T.

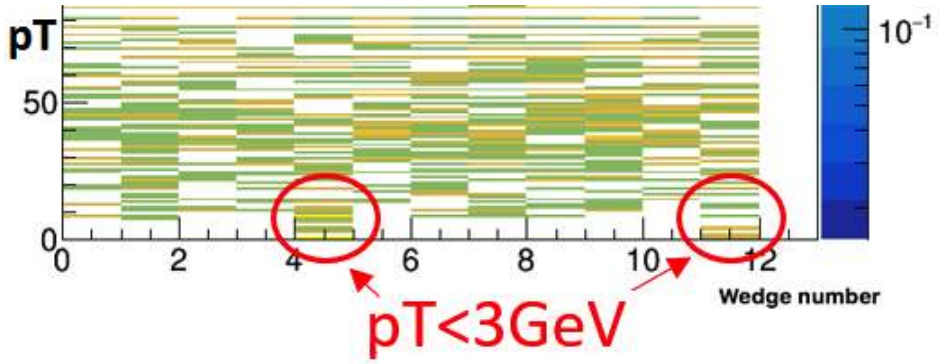


Figure 5.8: p_T per wedge processor histogram

It turned out that the cause of this symptom was a hardware issue in the FPGA BRAMs which was triggered by any phase change of the BRAM clock. The clock of the Level-1 Trigger systems is changing from local (CMS clock) to global (LHC clock) every time CMS is prepared for collisions and is reverted when the proton (or heavy ion) beam is dumped. It was decided, as a permanent solution, to automatically upload the firmware to the FPGAs of the BMTF cards each time the system is configured. This ensures that the effect of the change of the clock phase to the hardware LUTs is removed by the uploading of the firmware as this also reconfigures that BRAMs of the FPGA. After this solution was applied the comparisons of the emulator p_T versus the hardware p_T was satisfactory (Figure 5.9 right side).

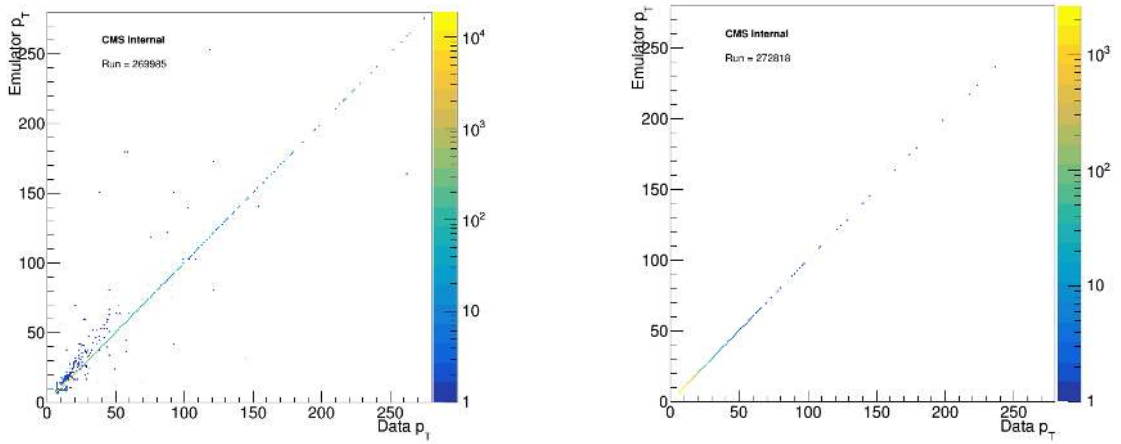


Figure 5.9: Fixing p_T corruption. On the left-hand-side plot the effect of corrupted data is shown. On the right-hand-side plot the symptom is gone.

5.4 Validation of the BMTF system after the commissioning

BMTF has been reviewed many times after the commissioning and many firmware problems and mistakes have been fixed. Input and output data of the BMTF are collected through the DAQ system. The inputs are used to feed a bit-to-bit emulator of the BMTF algorithm. The results of both BMTF system (data) and emulator where compared and presented in histograms.

5.4.1 BMTF Data/emulator comparisons using cosmic run

Table 5.1 presents the discrepancies of the BMTF output versus corresponding outputs of the emulator, for CMS runs taken using cosmic radiation. The agreement of the hardware system with the emulator is defined as a successful bit to bit comparison between the parameters of the hardware outputs with those of the emulator outputs. The agreement for the BMTF is over 95% which indicates that the system works as expected when is triggered in cosmic radiation runs (cosmics run).

RUN: 281214 Total muons 7186	**Number of Mismatches**	**Number of Mismatches/Total**	**Agreement %**
Number of muons	0	0	100.0%
p_T	3	0.000417478	99.96%
ϕ	297	0.0413304	95.87%
η	158	0.0219872	97.80%
Quality bits	4	0.000556638	99.94%
Track addresses	10	0.00139159	99.86%

Table 5.1: BMTF versus Emulator comarisons in cosmics run

The histograms presented in the Figure 5.10 show the comparisons of p_T, ϕ, η outputs of the BMTF system and the corresponding emulator parameters for 281214 cosmics run. The lower plots of the same Figure shows the data histogram (in black color) and the emulator histogram (in red color). The left side presents p_T results, the middle presents ϕ results and the right side presents η results.

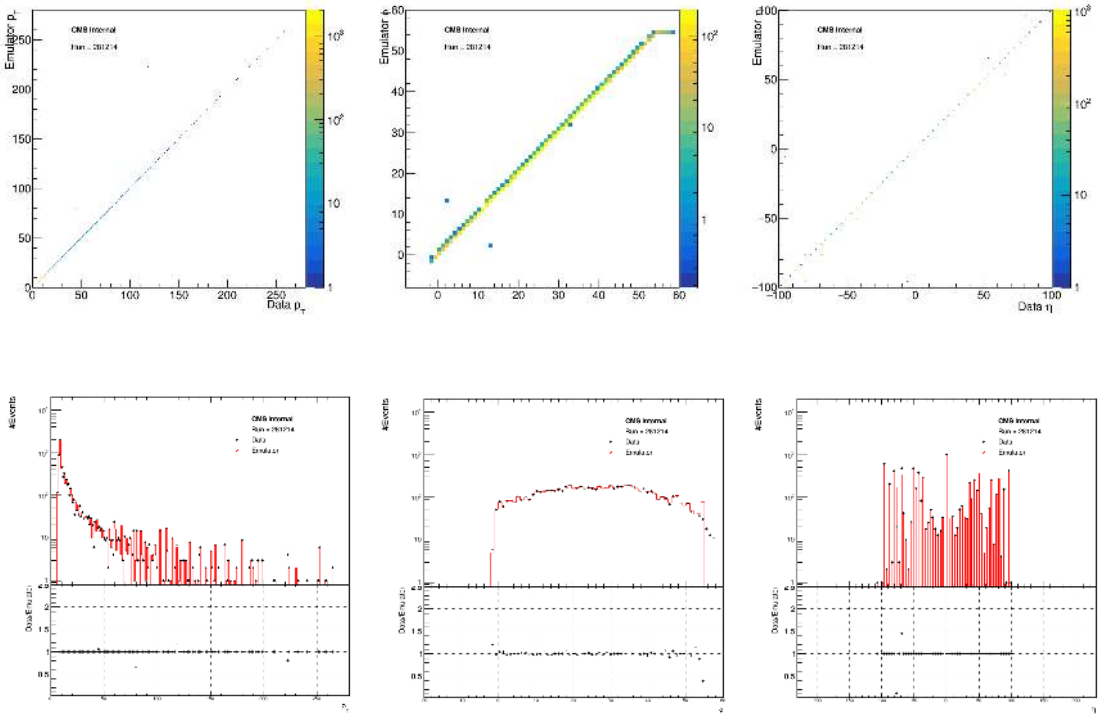


Figure 5.10: Muon properties in cosmics run. On the top histograms the vertical axis give the emulator parameters and the horizontal axis the hardware while on the bottom histograms the black is the hardware and the red the emulator values. Form the left to the right the corresponding histograms of p_T, ϕ and η are shown.

5.4.2 BMTF Data/emulator comparisons using pp collisions

As presented in table 5.2 the number of mismatches of the BMTF system, as compared with the BMTF emulator, is lower than 5% indicating a very good agreement between the hardware and the emulator. The data were taken from proton-proton collisions run 274094.

RUN: 274094 Total muons 1512	**Number of Mismatches**	**Number of Mismatches/Total**	**Agreement %**
Number of muons	15	0.0131694	98.68%
p_T	2	0.00132275	99.87%
Phi	63	0.0416667	95.83%
Eta	5	0.00330688	99.67%
Quality	10	0.00661376	99.34%
Track addresses	11	0.00727513	99.27%

Table 5.2: BMTF versus Emulator comarisons in pp collisions run

In Figure 5.11 the histograms of p_T, ϕ, η from collisions run 274094 are presented. The number of found muon candidates by the emulator versus those found by the BMTF system are presented in Figure 5.12. There are 15 mismatches out of 13612

which give agreement about 99.89%. The mismatches are not far away from the diagonal of the plot.

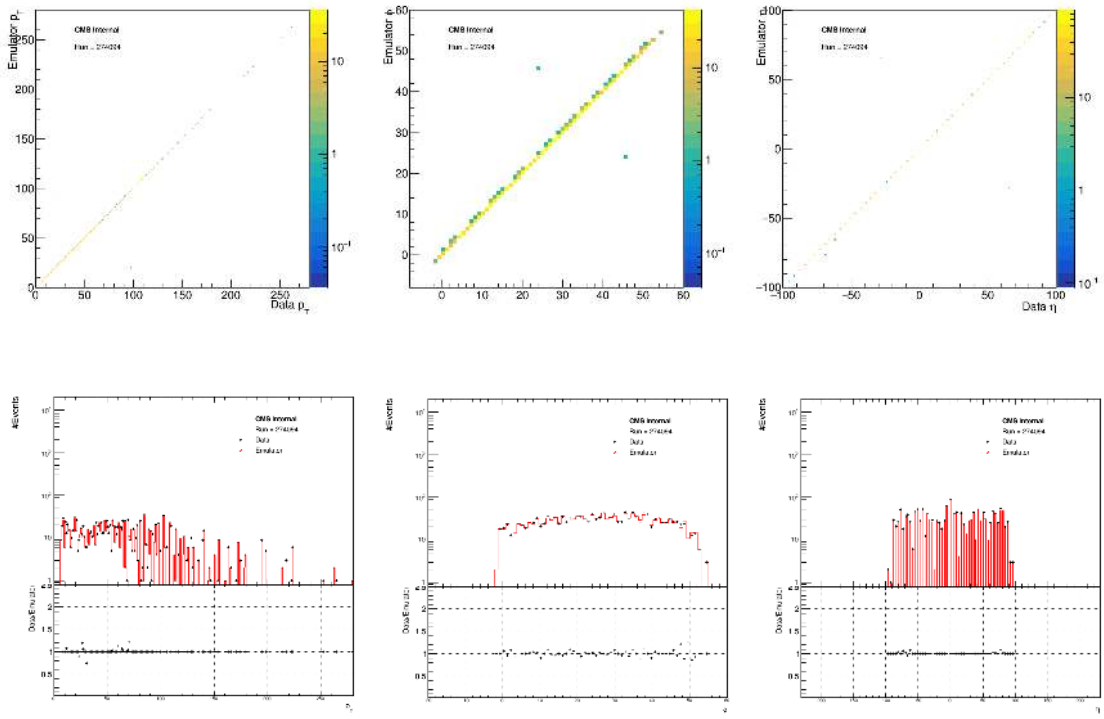


Figure 5.11: Muon properties in a p-p collision run. On the top histograms the vertical axis give the emulator parameters and the horizontal axis the hardware while on the bottom histograms the black is the hardware and the red the emulator values. Form the left to the right the corresponding histograms of p_T, ϕ and η are shown.

The remaining 0.1% discrepancies are due to known problems found in the ghost-busting (Subsection 4.1.4) VHDL block which has been fixed.

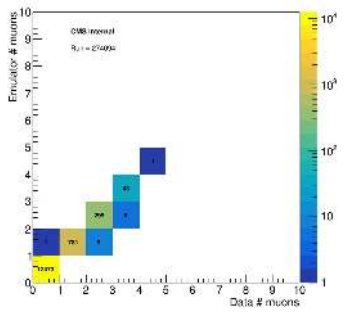


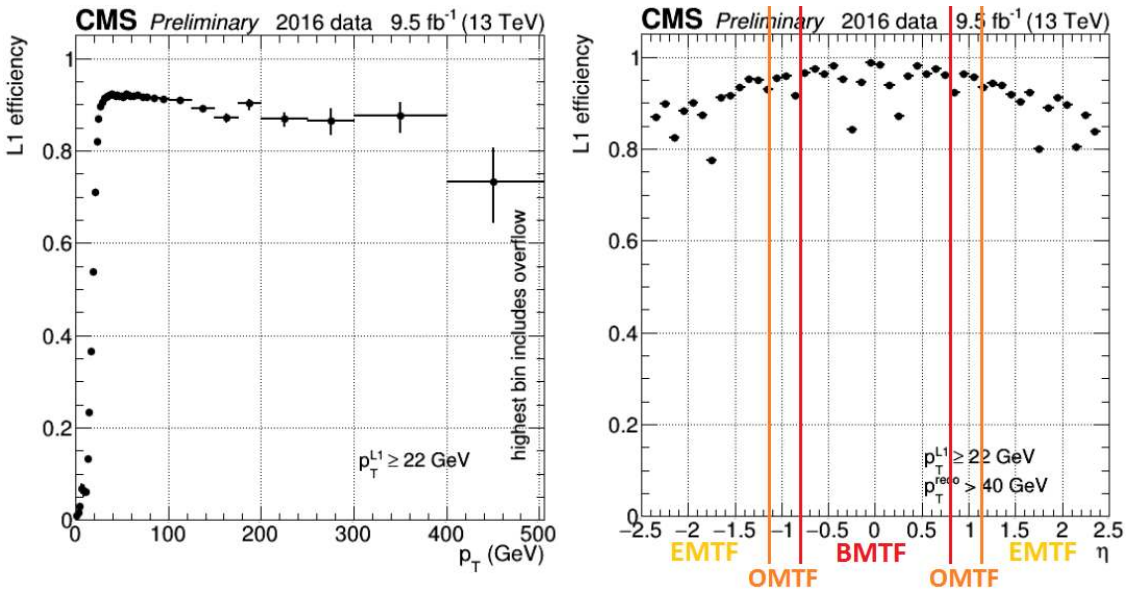
Figure 5.12: Number of muons found in the emulator versus BMTF system

5.5 Muon trigger performance

The barrel muon trigger upgrade of CMS Level1-Trigger took in place during the annual shutdown of LHC, the first quarter of 2016. As presented on this chapter BMTF successfully implemented and improved the algorithm was running in DTTF until the end of 2015. BMTF was fully commissioned before stable beams with p-p collisions delivered to CMS for 2016. The system run smoothly for 2016 and 2017 and data were collected to study the performance of the new muon trigger system.

5.5.1 Performance of muon trigger the 2016

The study of the muon trigger performance [4, 5] shows the efficiency of the muon trigger at a Level-1 transverse momentum cut of 22 GeV. On the left-hand-side of Figure 5.13, the p_T efficiency and on the right-hand-side the η efficiency are shown. As explained in chapter 4, the BMTF finds muon candidates within pseudorapidity $|\eta|$ <0.83, as shown in the central region of the rapidity plot of Figure 5.13b.



(a) p_T efficiency (b) η efficiency

Figure 5.13: L1 muon trigger performance

The plots of Figure 5.13, have been made using the tag and probe method [62] on a dataset collected with a single-muon trigger. The tag muons are defined as reconstructed muons with 0< $|\eta|$ <2.4, p_T >27 GeV and isolation <0.15 while the probe reconstructed muons as muons with 0< $|\eta|$ <2.4 and isolation <0.15.

5.5.2 Performance of muon trigger the 2017 and comparison with the legacy (2015) system

The muon trigger upgrade was completed in 2017, with the addition of combined DT+RPC trigger primitives from the TwinMux system in the barrel region, and RPC primitives from CPPF in the endcap. The upgraded system reduced the trigger

rate by a factor of two with respect to the legacy system, and slightly increased the overall trigger efficiency [63, 64].

Similarly to 2016 studies, Tag and probe selection for efficiency measurement was performed using single muon dataset with two offline reconstructed muons from 2017 data while detector conditions were certified as good. The tag muons are defined as reconstructed muons with $0 < |\eta| < 2.4$, $p_T > 30$ GeV, relative isolation < 0.15 and passing single muon isolated high-level trigger with dR(HLT, offline) < 0.3. The probe reconstructed muons were taken as muons with $0 < |\eta| < 2.4$, isolation < 0.15 and dR(tag, probe) > 0.5.

5.5.2.1 p_T efficiency for BMTF (tight L1 quality)

The efficiency versus p_T for the barrel track finder (including high-p_T muons) is shown in Figure 5.14. This plot shows the efficiency for the most common single muon trigger threshold (25 GeV) used in CMS analyses in 2017.

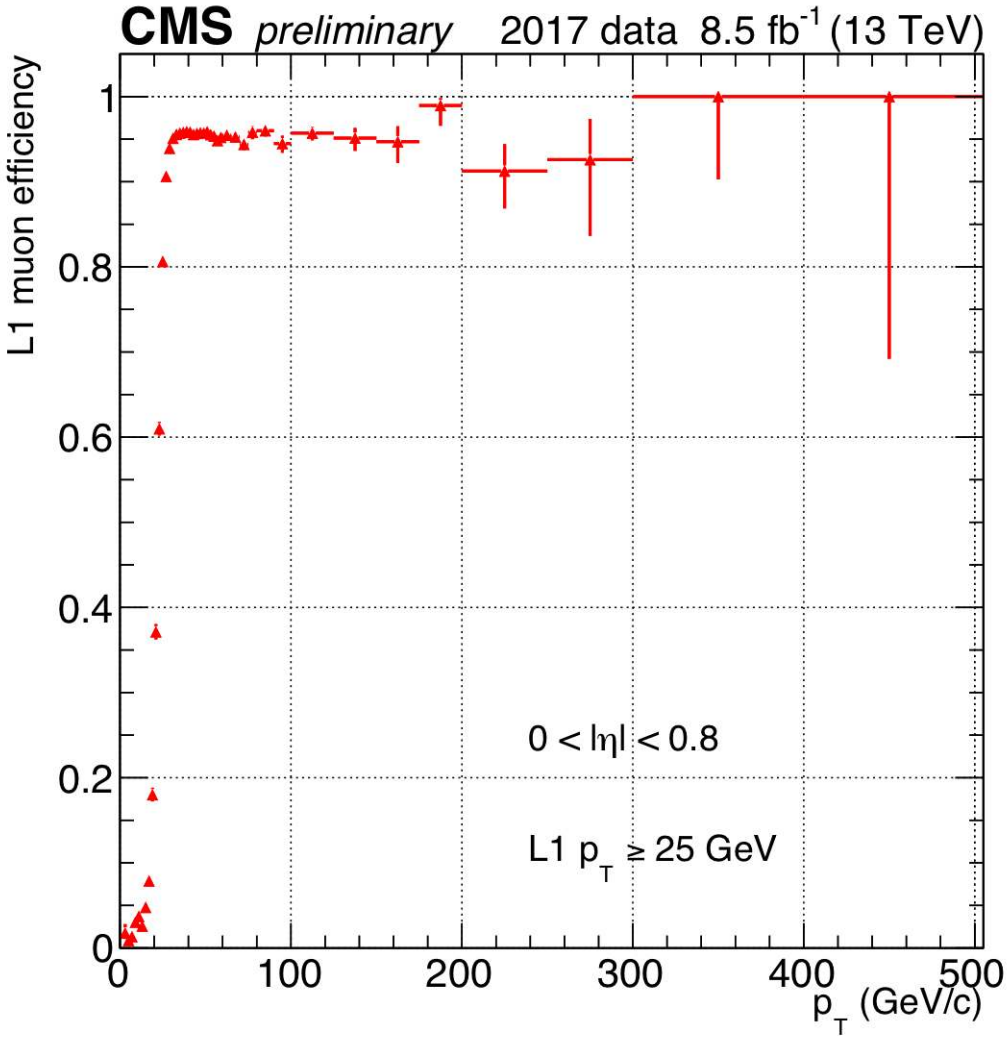


Figure 5.14: BMTF efficiency versus p_T.

5.5.2.2 BMTF and DTTF muon efficiencies

The following two plots compare the L1-Trigger muon efficiency of the upgraded barrel muon trigger (BMTF) with the legacy (DTTF). Figure 5.15 shows the efficiency versus p_T and Figure 5.16 the efficiency versus η where BMTF is within $|\eta|$ <0.8 limits. Reconstructed muons are defined with 0< $|\eta|$ <2.4 and 25 GeV threshold. The plots show similar trigger efficiency between the upgrade and legacy systems across the entire η range.

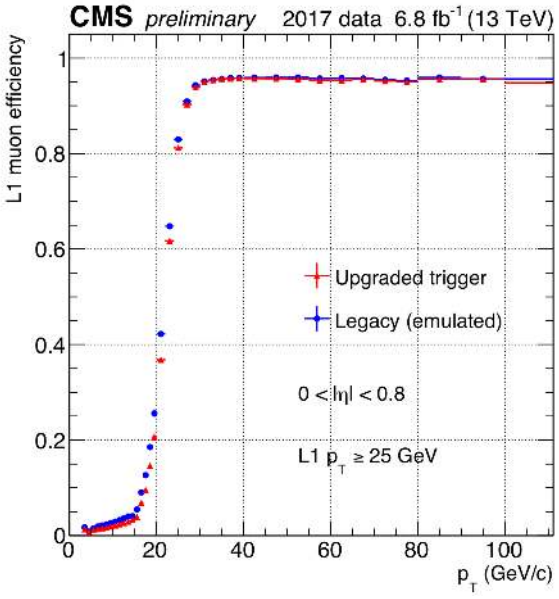


Figure 5.15: Barrel (BMTF) and legacy (DTTF) single Muon efficiency versus p_T.

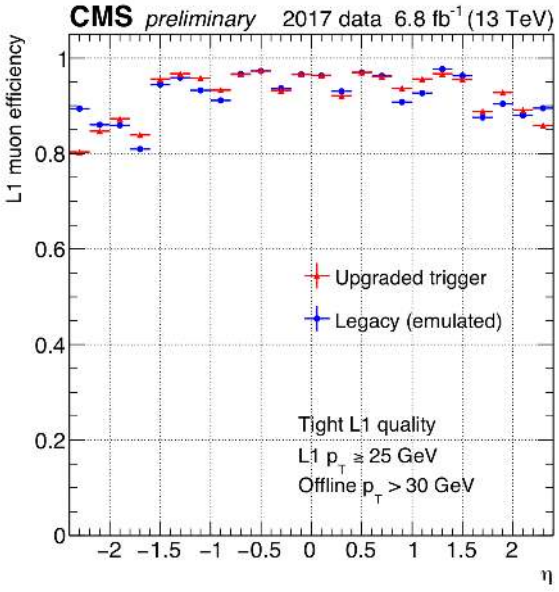


Figure 5.16: Barrel (BMTF) and legacy (DTTF) single Muon efficiency versus η.

5.5.2.3 BMTF and DTTF muon rates

The following two plots compare the muon trigger rates of the upgraded barrel muon trigger (BMTF) with the legacy (DTTF). Figure 5.17 shows the number of muons passing various p_T thresholds, built by the barrel muon track finder (BMTF) in the upgraded L1 muon trigger (2017), and compared with the emulated legacy trigger (2015), in arbitrary units. Figure 5.18 shows the distribution of muons per unit η passing a p_T threshold of 25 GeV, built by the BMTF in the upgraded L1 muon trigger (2017), and compared with the emulated legacy trigger (2015), in arbitrary units. As shown in plot of Figure 5.18, BMTF rate is about 40% lower than DTTF. Considering the rate deduction and the similar efficiency performance for the upgraded and legacy systems, it is concluded that BMTF is an improved system compared to DTTF.

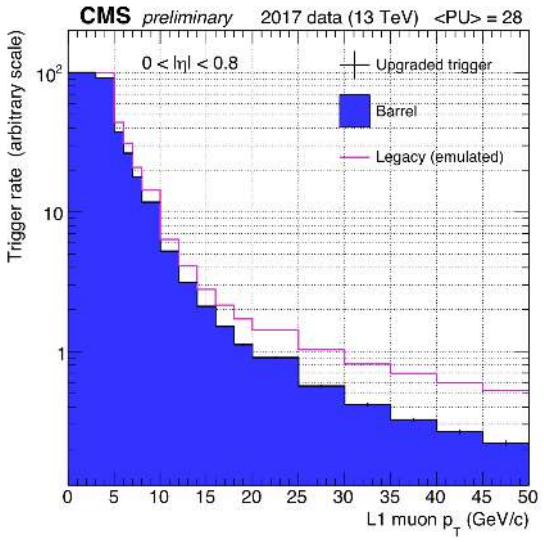


Figure 5.17: Barrel (BMTF) and legacy (DTTF) single Muon efficiency versus p_T.

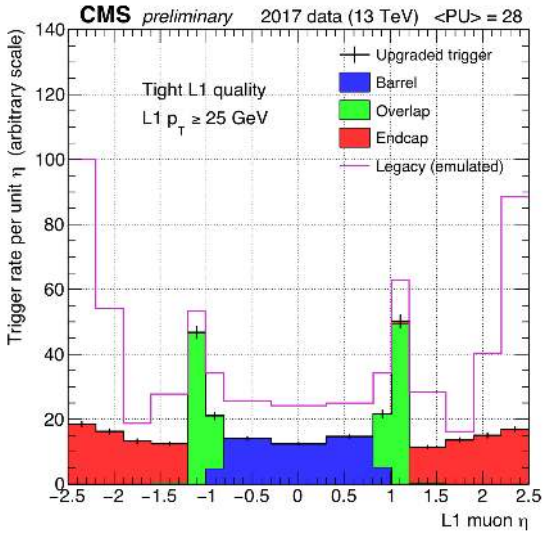


Figure 5.18: Barrel (BMTF) and legacy (DTTF) single Muon efficiency versus η.

Chapter 6

Control and Monitoring

As presented in chapter 3, the Level-1 Trigger is composed of a set of trigger processors and other general purpose boards, in μTCA format, interconnected by high-bandwidth serial links. Every trigger sub-system (like BMTF) is controlled and monitored using the online software through a framework called SoftWare for Automating the conTrol of Common Hardware (SWATCH). SWATCH provides a set of interfaces for controlling and monitoring the hardware of the upgraded Level-1 trigger system, following the common processor and the system models. The SWATCH provides a Graphical User Interface (GUI) cell to access the Level-1 sub-systems. The user using BMTF-SWATCH cell (top level in Figure 6.1) accesses all the AMC cards of the two crates of the BMTF system (12 MP7s, 2 MCHs and 2 AMC13s). The SWATCH cell provides configuration commands, status commands, monitoring flags and metrics plots to the user. With these commands the user can write or read registers or memories implemented in the firmware of the BMTF and AMC13 cards. The control/status registers as well as the monitoring block implemented in the firmware are presented in this chapter [65].

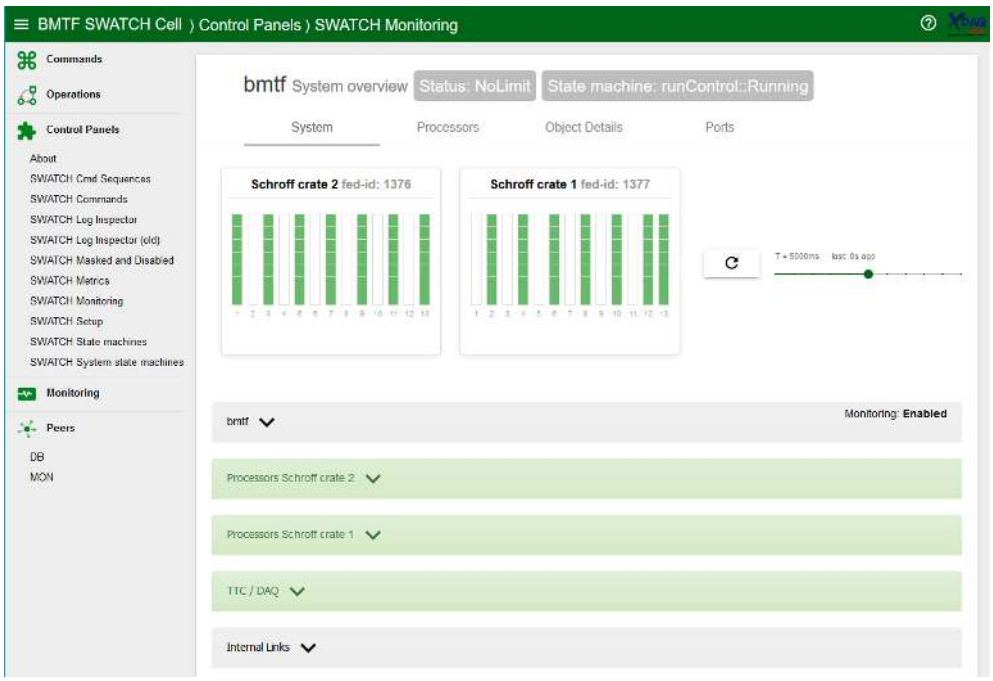


Figure 6.1: BMTF-SWATCH Cell top level

6.1 BMTF Control

The BMTF firmware follows the common MP7 framework controlled by the SWATCH. The firmware controls basic functions of BMTF system like: reset, align input links, masking channels and configure readout. Moreover, the system includes registers handled by the algorithm block. The values are loaded to the registers from a database every time a new run is started. Table 6.1, contains a list of control registers, their data width, the access permissions and a short description of its use.

Name	Bits	Mode	Description
Deserializer phase	3	R/W	Choose which phase of the six 240MHz domains to start decoding from
Mask Wheel N2	24	R/W	Masking input primitive of wheel -2 in station level
Mask Wheel N1	24	R/W	Masking input primitive of wheel -1 in station level
Mask Wheel 0	24	R/W	Masking input primitive of wheel 0 in station level
Mask Wheel P1	24	R/W	Masking input primitive of wheel +1 in station level
Mask Wheel P2	24	R/W	Masking input primitive of wheel +2 in station level
Overall quality cut	3	R/W	It applies a threshold to all quality bits of the input primitives
DT quality cut	3	R/W	It applies a threshold to the DT quality bits of the input primitives
RPC quality cut	3	R/W	It applies a threshold to the RPC quality bits of the input primitives
ETA odd reg.	1	R/W	Defines the eta stations orientation of the wheel 0 (right or left handed)
Open LUTs	1	R/W	Bypass the extrapolation LUTs to accept all the extrapolations
Disable new algo	1	R/W	Disables additional implemented algorithm (4.1.2.3 paragraph)
Manual sorting	12	R/W	Bypass muon sorting and choose a manual output order

Table 6.1: BMTF - algorithm control registers

Mask wheel N2, N1, 0, P1 and P2 registers apply masking to the inputs of BMTF algorithms in a station level. During cosmics runs all inputs stay unmasked because cosmic rays give low trigger rate (about 100 Hz) and the system collects information only for testing. During collisions the first station (MB1) of wheels ±2 in all wedges are masked. This masking reduces the muons found twice (ghost muons) from BMTF and OMTF sub-systems. As shown in Figure 6.2, MB1 of wheel +2 is totally covered by the OMTF subsystem and therefore it is not included to the BMTF system. The station is excluded from BMTF during collisions.

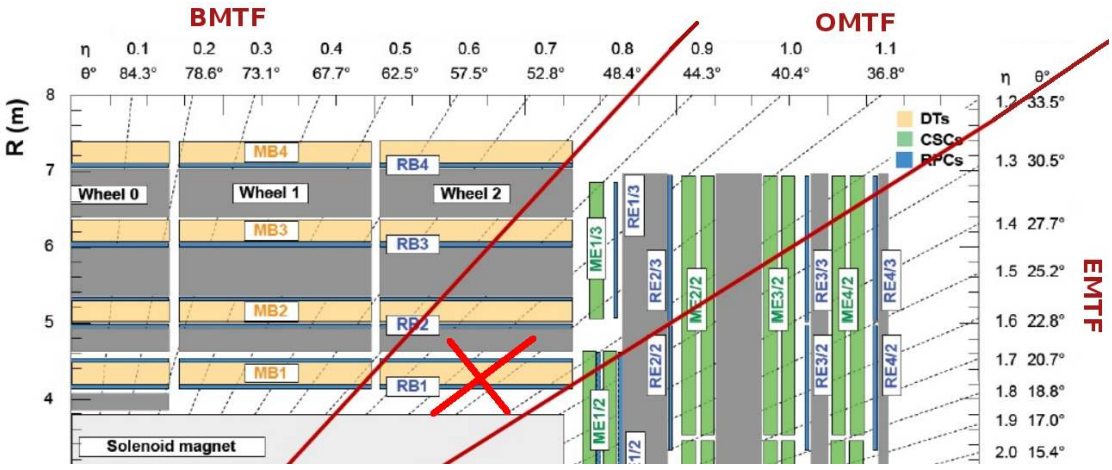


Figure 6.2: BMTF 1st stations of wheels |2| are masked during collisions.

The ETA chambers of wheel 0, have different orientation for odd and even numbers of wedges [66]. In case of wrong definition, the η track finder, indicates tracks with revered η values. To compensate that, and since in all processors use the same algorithm, a register on each algorithm defines the orientation of the η registers

in wheel 0. This *ETA odd* register value is part of the configuration of BMTF card and is loaded from a database.

Under normal running conditions of the BMTF system, all configuration registers except from *ETA odd*, *Mask* and *ETA* control take the default values (zeros). The default values ensure no quality threshold, for the inputs and normal sorting of the found muon tracks. The additional ϕ algorithm described in the Section 4.1.2.3, is enabled by default, but it can be disable, if requested, by the *Disable new algo* register. The *Deserializer phase* register select one of the six phases of the LHC clock (40 MHz), used by the logic to deserialize the input data frames, running in 240-MHz domain (six times higher than the LHC clock). Finally, *open LUT* register is able to bypass the extrapolation logic of the algorithm and forces it to accept all tracks.

6.2 BMTF monitoring

BMTF sub-system contains monitoring blocks, i.e. simple up-counters, implemented to increase the register values when a signal is true. The signals are driven by input block of the algorithm, by output block of the PHTFs and by the output of the Wedge Sorter. Table 6.2 shows the status register which is accessed by the online software which uses them to issue warning or error flags in case of higher-than-a-threshold value. The Sample trigger rate of the monitoring blocks is controlled by the *Sample rate* register. A value of 100 correspondents to 40 MHz.

Register Register name	**Vector**	**Bits**	**Mode**	**Description**
Sample rate	1	12	R/W	Defines the sampling rate in the monitoring counters
p_T threshold	1	9	R/W	Applies threshold between hi and low p_T muons counters
DT rate	20	24	RO	DT input data rate per stations (1,2,3,4) and wheel (-2,-1,0,+1,+2)
DT corr	20	24	RO	DT correlation input data rate per stations (1,2,3,4) and wheel (-2,-1,0,+1,+2)
RPC rate	20	24	RO	RPC input data rate per stations (1,2,3,4) and wheel (-2,-1,0,+1,+2)
PHTF Q rate	84	24	RO	Sector output data rate by quality bits (1,2,3,4,5,6,7) per muon (1st,2nd) as well as per wheel (-2,-1,-0,+0,+1,+2)
PHTF p_T rate	24	24	RO	Sector output data rate by p_T per muon (1st,2nd) as well as per wheel (-2,-1,-0,+0,+1,+2)
ETTF rate	12	24	RO	ETA Sector output data rate per muon (1st,2nd) as well as per wheel (-2,-1,-0,+0,+1,+2)
WS Q rate	21	24	RO	Wedge sorter data by quality rate per muon (1st,2nd,3rd) as well as per wheel (-2,-1,-0,+0,+1,+2)
WS p_T rate	6	24	RO	Wedge sorter data muon (1st,2nd,3rd) per p_T threshold (hi,low)

Table 6.2: BMTF-algorithm status registers

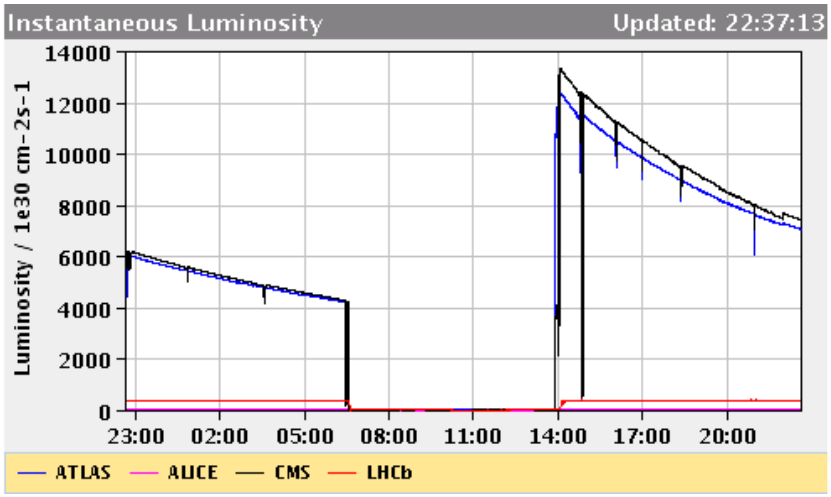
The BMTF uses the status registers listed in Table 6.2. Registers: *DT rate*, *DT corr* and *RPC rate* indicate the rate of Trigger Primitives (TP) at the input of the BTMF processor card for every station. *DT rate* is a vector of registers that indicates the rate of DT data. Respectively to this vector, *DT corr* gives the rate of DT correlated data and *RPC rate* of RPC data. Two vectors of *PHTF* status registers give the track finder rate of the PHTF algorithm. The *PHTF Q* sorts by quality bits and *PHTF* p_T by high and low p_T. The threshold between the high and the low p_T is defined by p_T *threshold* register. The vector of registers: *ETTF rate* give the η track finder rate on every wheel: two muons on each wheel. *WS Q rate*

is a register vector that gives the output trigger rate of the first, second and third muon candidates of the BMTF, ranked by quality (1, 2, 3, 4) and finally *WS p_T rate* is a register vector that gives three muons racked in high and low p_T according to the applied threshold.

6.2.1 Barrel-trigger rates

The behavior of the BMTF system is stable as it has been recorded using the monitoring registers, presented in the previous Section. Figure 6.3a shows the output rates of the twelve BMTF processors, expressed by the 1st Hi *WS p_T rate* register of each BMTF card. Figure 6.3b shows the instantaneous luminosity in ATLAS, ALICE, CMS and LHCb experiments. As shown in the plot CMS curve (black color) starts from 13,000 x 10^{30}cm$^{-2}s^{-1}$ and falls smoothly. This is the maximum luminosity value for 2016 as in CMS 2,220 bunches were colliding.

(a) BMTF output rate of all processors (1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12)

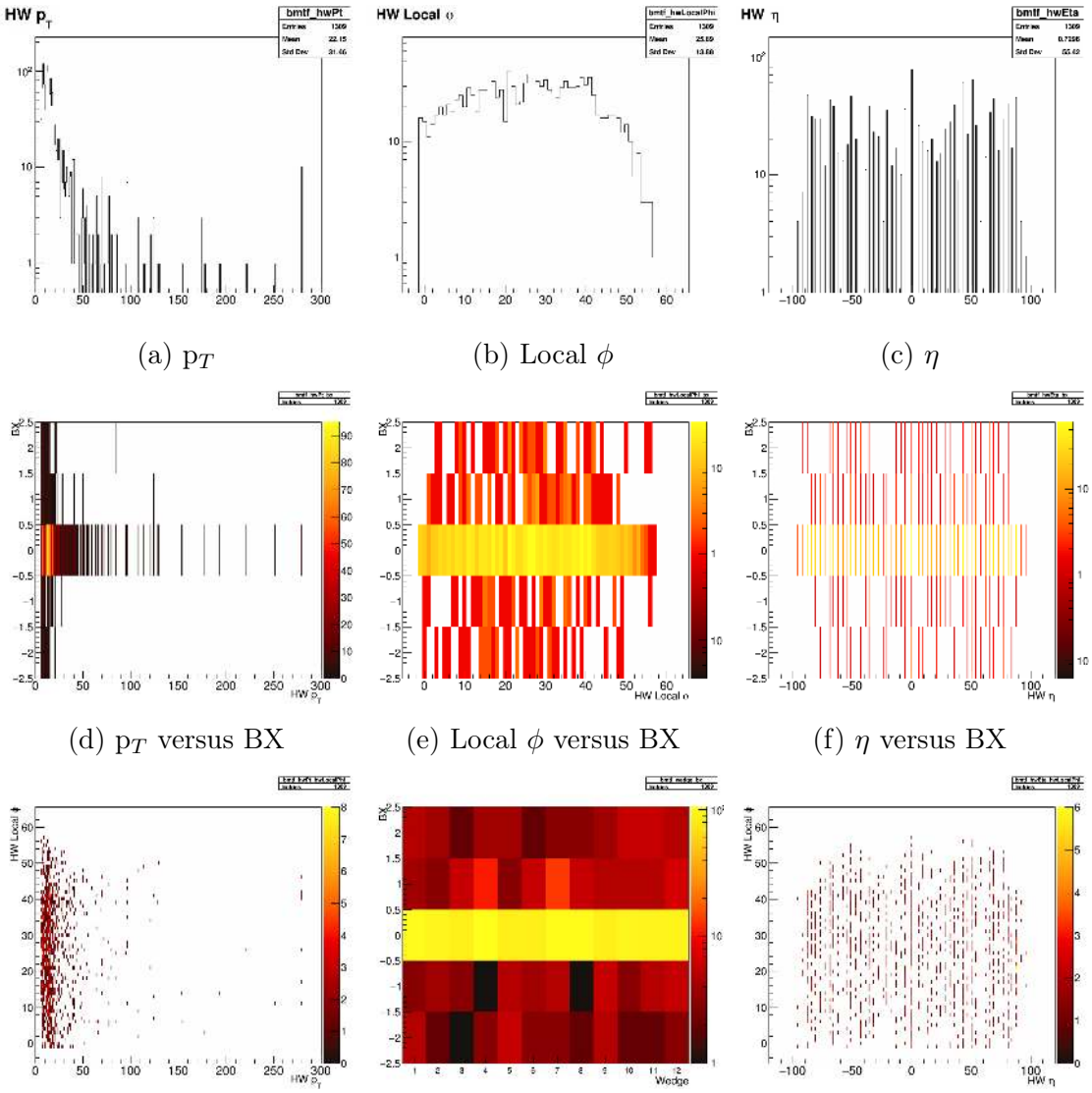


(b) Luminosity with 2,220 colliding bunches in stable beams

Figure 6.3: Luminosity and BMTF trigger rate

There is a big drop in the beginning of the stable beams and few drops later. All drops are caused by beam scanning calibrations which are happening at regular basis during a collision run. BMTF trigger rate is falling as well, as it experiences the drops of the beams. The time evolution of the BMTF processors trigger rate is similar to the luminosity time evolution. This indicates a smooth functioning of the BMTF system.

6.3 Online Data Quality Monitoring



(a) p_T (b) Local ϕ (c) η

(d) p_T versus BX (e) Local ϕ versus BX (f) η versus BX

(g) p_T versus local ϕ (h) Wedge triggers versus BX (i) η versus local ϕ

Figure 6.4: DQM - evaluation histograms of BMTF from the collision run 274094. Top left: p_T distribution, top middle: */phi* distribution, top right: η distribution, center left: p_T versus bunch crossing (-2, -1, 0, 1, 2), center middle: ϕ versus bunch crossing, right middle: η versus bunch crossing, bottom left: p_T versus ϕ, bottom center: trigger rate versus bunch crossing, bottom right: η versus ϕ

Data Quality Monitoring (DQM), is a central tool in the CMS experiment [67] providing live evaluation of BMTF. The DQM software collects the data from the subsystems and fills histograms which are monitored real-time by control-room personnel. The histograms show the quality of the running systems as they make visible any eventual "hot spot". The "hot spot" in a histogram indicates unusual overflow high-rate spot that is caused by an instability in the referred sub-system. Figure 6.4, presents the online DQM of BMTF running under collisions. Plot 6.4h shows the Wedge processors trigger rate (x-axis) versus the bunch crossing (BX) time (y-axis). The plot indicates that all BMTF cards mostly trigger in the nominal time BX=0.

No anomalous plot is shown in the DQM of the BMTF, fact that indicates a smooth running.

Chapter 7

Implementation of logic blocks among L1-trigger sub-systems

Most of the Level-1 Trigger subsystems require the use of similar logic blocks for similar functionality. For example as presented in Chapters 3 and 4, the BMTF asynchronous 10-Gb/s protocol is used to receive trigger primitives from TwinMux cards. This fact was the motivation to use the MP7 set of logic blocks in the TwinMux in order to benefit from the modular VHDL design of the MP7 and avoid solving related problems, already found and fixed in the MP7 logic blocks. Instead of "rediscovering the wheel", the MP7 asynchronous 10-Gb/s protocol as well as the rest MP7 set of logic blocks have been used in order to create a minimal and modular design, used to build logic blocks for the FPGAs of TwinMux as well as other Level-1 subsystems. Similar firmware logic blocks have been generated for the TwinMux, the CPPF and the AMC502 FPGAs. Figure 7.1 shows the setup used for testing the generated logic blocks on those cards. The crate contains also one MP7, used to evaluate the reference minimal MP7 logic blocks design. One more MP7 is used as receiver card in order to validate a successful data transaction from the testing cards. The patch panel shown on the top of the photograph is used to interconnect the outputs of the testing card with the inputs of the MP7 used to validate the data transactions. The test is consider successful when the MP7 is locking the input links.

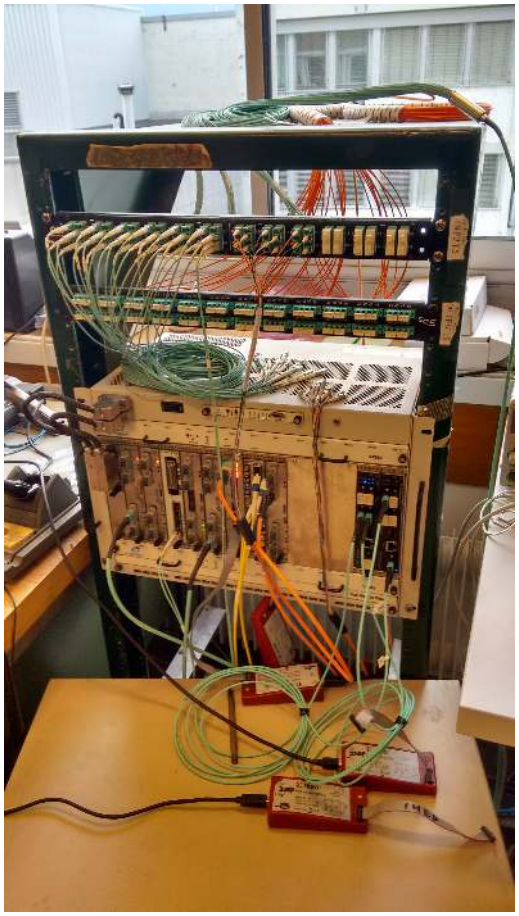


Figure 7.1: Electronics setup for the testing of the TwinMux, CPPF and AMC502

Figure 7.2 shows the patch panel and the connected optical fibers running the asynchronous 10-Gb/s links. On the rear side of the patch panel an other MTP-48 cable connects it with the MP7 board which validate the transactions. Shown on the left of the Figure, LC cables connect the patch panel to the outputs of the MP7 card running the implemented logic blocks. In the middle, the LC cable is connected to the mezzanine card of the AMC502 running the generated logic blocks. On the right side a MTP-12 cable is shown. This cable is connected to the TwinMux or CPPF, both running the generated logic blocks.

Figure 7.2: Patch panel connections of MP7, TwinMux, CPPF and AMC502 cards

The logic blocks of the FPGAs used in the TwinMux, CPPF and AMC502 subsystems are designed such as they can easily be edited in order to follow any upgrade of the reference VHDL blocks of the MP7 design.

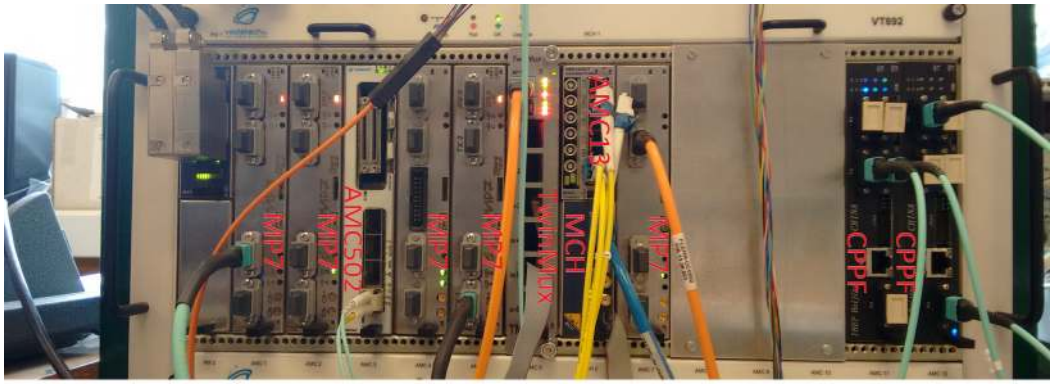


Figure 7.3: μTCA test-bench hosting 6 MP7s, 1 TwinMux, 2 CPPF and 1 AMC502

Table 7.1 presents the utilization report of the FPGA (*XC7VX690TFFG1927-2*) resources for the MP7 minimal design, implemented using the logic blocks from the MP7 reference design. This report occurred after removing VHDL blocks referred to specific MP7 on board components that MP7 hardware accesses. The removed logic blocks are I^2C interface and control of Xpoint switch and MMC contention, SPI interface which reads the status for the minipod optics and parallel interface for connecting which interconnect the FPGA with an external mezzanine. The remaining logic block contains:

- Clock management and fabric distribution
- IPbus implementation and control logic

- TCDS decoding and control logic
- Asynchronous 10-Gb/s protocol
- Channel buffers instantiation
- DAQ protocol and readout packaging

Resource	Used	Available	Utilization %
LUT (LookUp Table)	98,296	433,200	**22.69**
LUTRAM (LUT Random Access Memories)	8,607	174,200	**4.94**
FF (Flip Flops)	92,176	866,400	**10.64**
BRAM (Block of RAMs)	328	1,470	**22.31**
IO (Standard Inputs and Outputs)	16	600	2.67
GT (Gigabit Transceivers)	74	100	74.00
BUFG (Generic Buffers)	6	32	18.75
MMCM (Mixed Mode Clock Manager)	3	20	15.00

Table 7.1: Post implementation report of a minimal MP7 design

This minimal logic block design was the baseline from where similar logic blocks were generated and used in the FPGAs of the cards (TwinMux, CPPF and AMC502) shown in Figure 7.3.

7.1 VHDL logic blocks for TwinMux FPGA

The *XC7VX330TFFG1761-3* used in the TwinMux card is a middle-size speed-grade 3, Virtex-7 FPGA. It has 7 Multi Gigabit Transceiver (MGT) BANKs of (1 BANK contains 4 transceivers). BANK #117 - #119 are used for high data-rate links and #115 for the DAQ and TCDS links. The TwinMux application requires 3 BANKs (12 links) and the related logic, running the 10-Gb/s asynchronous protocol. The hardware components used to implement this protocol and the related logic are shown in the Figure 7.4 in yellow color. TwinMux FPGA has totaly 14 BANKs, 2 (X1Y2 and X1Y3) includes all the rest blocks. The blue color in the Figure shows the distribution of the readout logic over the FPGA die and the green all the rest logic which is constrained to BANK X1Y2 and include IPbus protocol, control and status handled via IPbus, TCDS decoding and clock management blocks. Table 7.2, lists the set of the logic blocks resource utilization of the TwinMux. As is shown, 14 transceivers (MGT) are used for

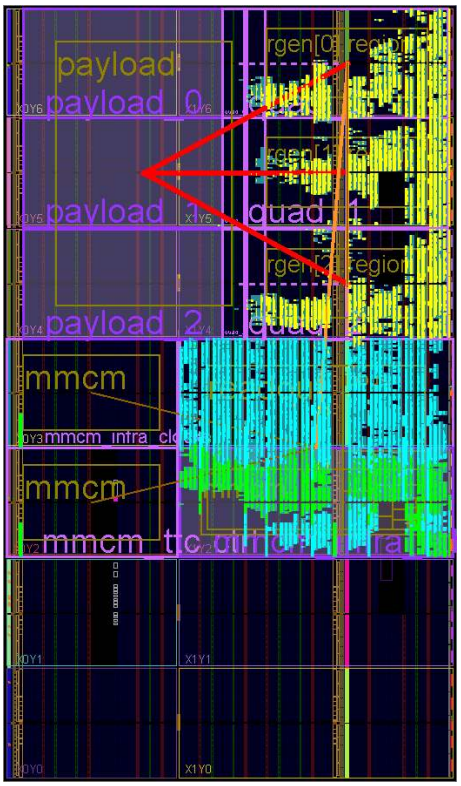


Figure 7.4: TwinMux post implementation RTL distribution

the implementation of the 12 I/O, 1 IPbus and 1 DAQ link. The design includes the top level of the TwinMux logic and leaves more than 85% of the resources unused in order to implement logic to serve the DT TPG links running at 480 Mb/s and the RPC and HO TPG links running GOL at 1.6 Gb/s. In addition a part of the "free" resources are reserved to implement the super-primitives logic block as described in 3.1.2.1 and additional DAQ logic to collect the data of the input links and send them to the readout chain.

Resource	Used	Available	Utilization %
LUT	29,835	204,000	**14.62**
LUTRAM	8,475	70,200	**12.07**
FF	25,295	408,000	**6.20**
BRAM	100	750	**13.33**
IO	14	700	2.00
GT	**14**	28	50.00
BUFG	7	32	21.88
MMCM	3	14	21.43

Table 7.2: Post-implementation report of TwinMux base firmware

7.2 VHDL logic blocks for CPPF FPGAs

In contrast with the MP7 projects, in CPPF the set of logic blocks is divided in two separate FPGAs (Subsection 3.1.2.2).

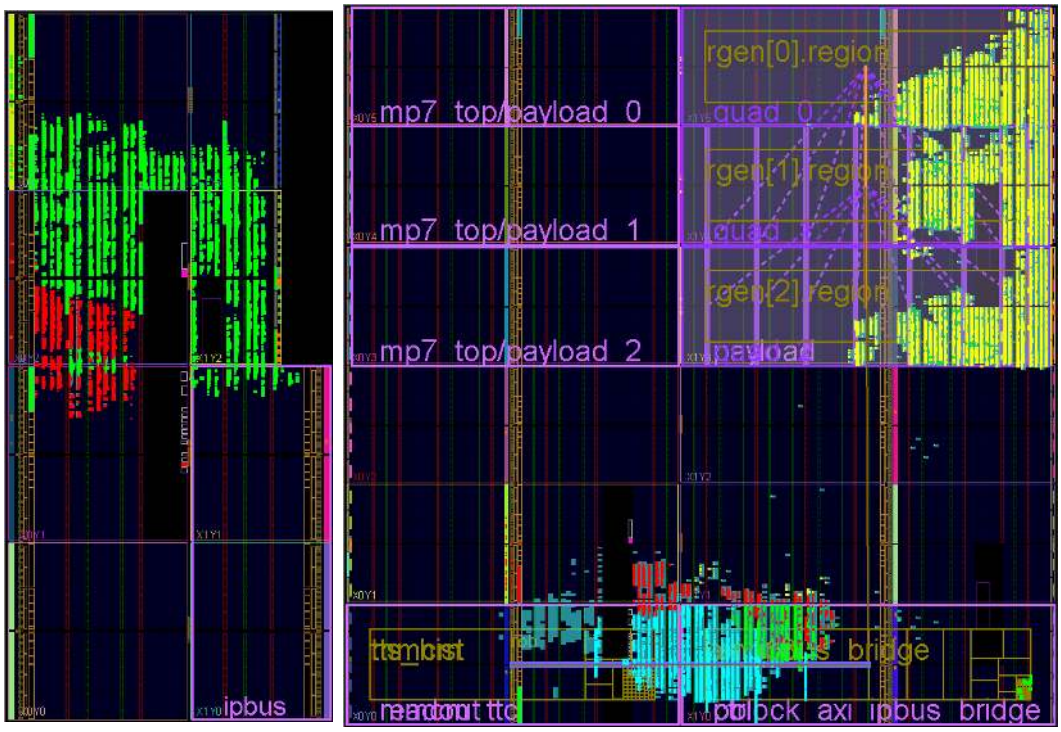


Figure 7.5: Post-implementation floor plan of the CPPF card FPGAs: Left Control Kintex-7, right: Core Virtex-7

The first named "control" FPGA, is a Kintex-7 *XC7K70TFBG484-2* and includes the IPbus interface using 1 transceiver of the BANK 115 as well as a control/status logic (showing with green color in the left hand side of the Figure 7.5) and a master chip2chip IP-core used to control the Virtex-7 FPGA "core" FPGA *XC7VX415TFFG1158-2* (showing with red color on the right hand side of Figure 7.5).

The post-implementation result on the two FPGAs are shown in Figure 7.5. On the right hand side the implemented logic of the "core" FPGA, includes 3 BANKs running 12 asynchronous 10-Gb/s links (exactly as in the TwinMux) and is shown in yellow color. BANKs #117 - #119 are used for the high data-rate links. In the same Figure the implementation of a chip2chip slave and the IPbus-UDP cores are show in red color. Those logic blocks interconnects the Virtex-7 with the Kintex-7. On the same Figure, green color represents the hardware elements of the FPGA used by the TCDS decoding logic and the Mixed-Mode Clock Manager (MMCM) logic. Finally, in light blue color, the corresponding elements of the readout (DAQ) logic are shown.

Table 7.3, shows the post-implementation results after porting the minimal MP7 set of logic blocks to the two FPGAs. The report of Table 7.3, shows that a small part of the Kintex-7 and Virtex-7 resources is used. Core FPGA implements 12 + 1 links (GT) for the asynchronous protocol and the readout. Control FPGA uses 1 transceiver with 1GbE and IPbus.

Resource	**Used**	**Available**	**Utilization %**
LUT	5,751	41,000	**14.03**
Memory LUT	134	13,400	**1.00**
FF	8,428	82,000	**10.28**
BRAM	22.5	135	**16.67**
IO	27	285	9.47
GT	**1**	5	20.00
BUFG	14	32	43.75
MMCM	1	6	16.67
PLL	2	6	33.33

Resource	**Used**	**Available**	**Utilization %**
LUT	21,450	257,600	**8.33**
Memory LUT	2,398	104,400	**2.30**
FF	18,906	515,200	**3.67**
BRAM	69.5	880	**7.90**
IO	29	350	8.29
GT	**13**	60	21.67
BUFG	13	32	40.62
MMCM	2	12	16.67
PLL	2	12	16.67

Table 7.3: Post implementation report of the two FPGAs. On the top: "control" Kintex-7 FPGA, on the bottom: "core" Virtex-7 FPGA

The unused hardware resources of the core FPGA cover all needs of the algorithm block as well as requirements of the RPC receiver block (GOL links) running at 1.6 Gb/s. Algorithm processes the RPC TPs, forms clusters and send them to the EMTF subsystem using the asynchronous protocol [38].

7.3 VHDL logic blocks for AMC502 FPGA

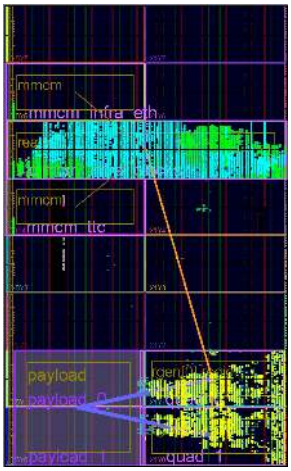


Figure 7.6: AMC502 post implementation RTL distribution

The commercial AMC502 described in Section 3.1.3, hosts the large scale Kintex-7 *XC7K420TFFG1156-2* FPGA. In contrast to the rest of trigger subsystems in CMS that use GTH transceivers, AMC502 uses GTX transceivers. The firmware developed for AMC502 FPGA requires the replacement of the GTH logic blocks used for the 10-Gb/s asynchronous, 1-Gb/s IPbus and DAQ links, with GTX logic blocks. Figure 7.6 shown the implemented logic blocks which contain the infrastructure logic (green color), the readout logic (blue color) and the 8 x 10-Gb/s asynchronous links in the MGT BANKs 111 and 112. Table 7.4, present the post-implementation report and the usage of the Kintex-7 resources. The transceivers of the 2 GTX QUADs (BANKs 111, 112) are used for the high data-rate links to SFP+ optics connected in a high-speed mezzanine mounted in the 1st FMC of the AMC502 carrier (Figure 7.7). The second low-speed mezzanine is used to receive LDVS parallel signals for the RPC detectors running at 40 Mb/s.

Resource	**Used**	**Available**	**Utilization %**
LUT	28,274	260,600	**10.85**
LUTRAM	8,482	108,600	**7.81**
FF	21,915	521,200	**4.20**
BRAM	104	835	**12.46**
IO	24	400	6.00
GT	**10**	32	31.25
BUFG	9	32	28.13
MMCM	3	8	37.50

Table 7.4: Post-implementation report of AMC502 design

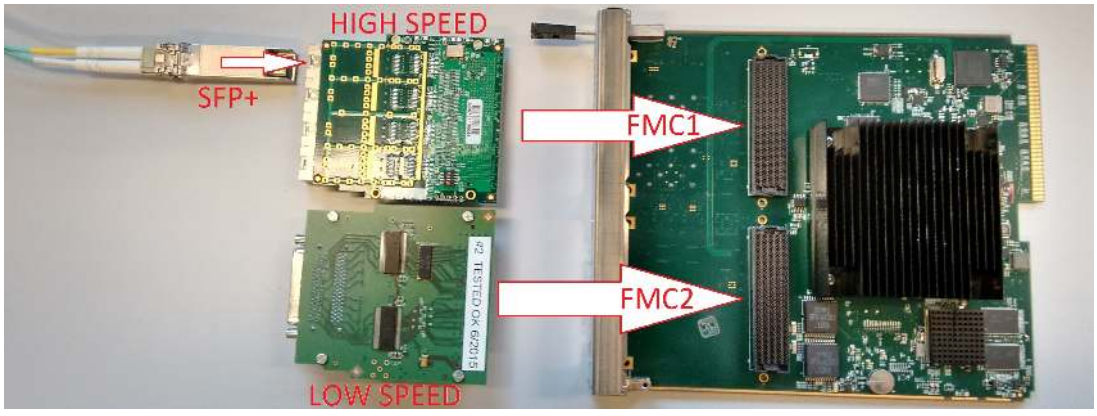


Figure 7.7: AMC502 card, the high and low speed mezzanine modules and the SFP+ optic

Apart from the minimal set of logic blocks, the implemented logic contain receiver blocks in order to capture the LVDS inputs. While the input data rate is 40 MHz,

the receivers over-sample the data using 240-MHz clock. Then the logic identifies the data critical meta-stability point and move the sampling point far from it to ensure no data corruption. Then it sends the data to μGT using the 10-Gb/s asynchronous protocol.

The firmware is modular. By changing few parameters, the user can extend the logic and instantiate 16 instead of 8 GTXs, which will make the design use 10-Gb/s asynchronous on both FMCs (Figure 7.7).

7.4 Porting VHDL framwork to FPGAs of developmant cards

The motivation of porting the MP7 minimal set of logic blocks to the FPGAs of the development boards described in the following Sections 7.4.1 and 7.4.2 was the need to design of VHDL blocks for the AMC502 before the hardware was available. Moreover KC705 and VC707 development boards have similar FPGA architectures as the FPGA of the AMC502 and provide data and clocking I/Os in order to build a test-bench and validate the set of logic blocks. The work described in this Section, initially launched in order to cover a fallback muon trigger plan which requires triggers from the old regional muon Level-1 Trigger carried in LVDS signals to be transformed to 10-Gb/s links forwarded to μGMT. After the upgraded system proved reliable it was decided that the fallback plan is not needed and the AMC502 set of logic blocks used in μGT as mentioned in Section 3.1.3.

7.4.1 Porting VHDL set of logic blocks to KC705 FPGA

The setup shown in Figure 7.8 hosts the KC705 development board.

Figure 7.8: KC705 - Developing fallback for the muon trigger

It uses the same FMC mezzanine with SFP+ as in the AMC502 application and includes, an CDCE low jitter clock generator to feed the GTX reference clock and an

ethernet connection to establish IPbus interface via BASE-X or external PHY chip. KC705 hosts the *XC7K325T-2FFG900C* Kintex-7 [68]. This FPGA has the same architecture as the one used in the AMC502 but has less resources. The KC705 set of logic blocks is based in the minimal MP7 set of logic blocks and implements the 10-Gb/s asynchronous protocol as well as the rest of the logic implemented later in the AMC502. KC705 design is accessible by IPbus and controlled by a PC. Loopback test has shown a reliable system running with 2 implemented GTX BANKs.

7.4.2 Porting VHDL set of logic blocks to VC707 FPGA

The setup shown in Figure 7.9 hosts the VC707 development card [69]. It uses the same FMC F14 from Faster Technology with SFP+ as in the AMC502 application and includes a low jitter 40-MHz clock source connected to on board SMA and an Ethernet connection to establish IPbus interface via BASE-X. Also it has the FMC XM105 which is connected with loopback ribbon cables in order to feed the framework inputs with 64 low speed LVDS signals as in AMC502. The board provides High Pin Count (HPC) FMCs that give the ability to loopback test patterns. Also the VC707 hosts the *XC7VX485T-2FFG1761C* Virtex-7 FPGA providing GTX transceivers as the FPGA of the AMC502.

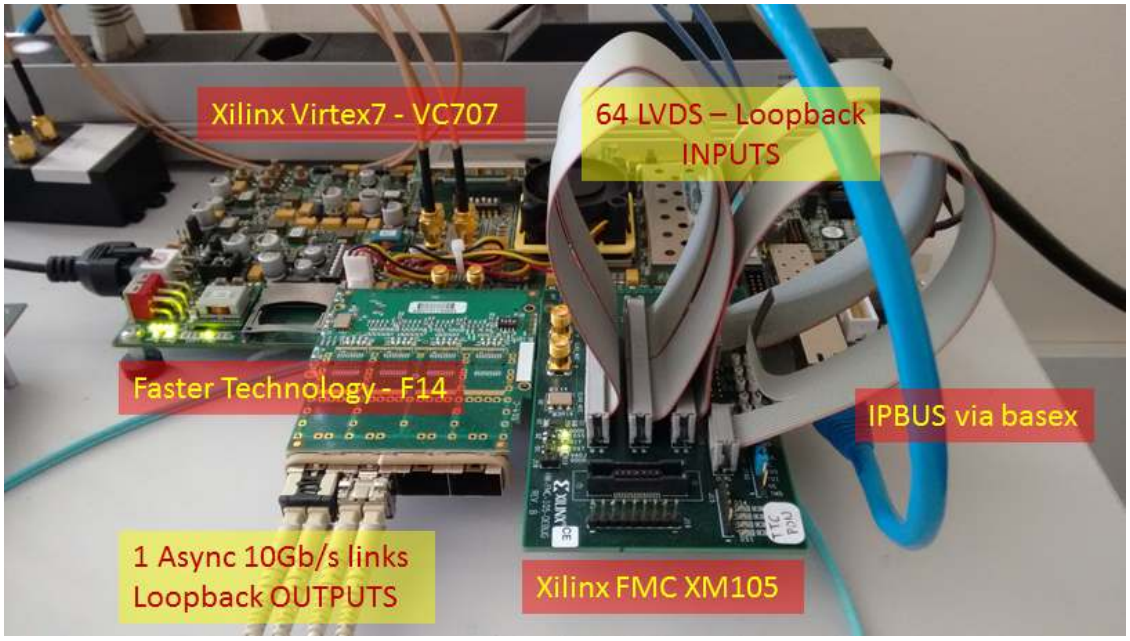


Figure 7.9: VC707 - Developing fallback for the muon trigger

The test bench includes:

- A frame generator running at 40 MHz that provides random patterns
- A configurable delay logic that adds latency to the generated patterns (emulate the cable delay)
- Buffer I/Os to connect cables and loopback the data
- A Finite State Machine (FSM) that automatically chooses the "best" phase of the sampling clock of receive the input data.

- A frame checker that increases an error counter when the input has any bit error
- The logic blocks getting the input-data frames and forward them to the optical links running 10-Gb/s asynchronous protocol.

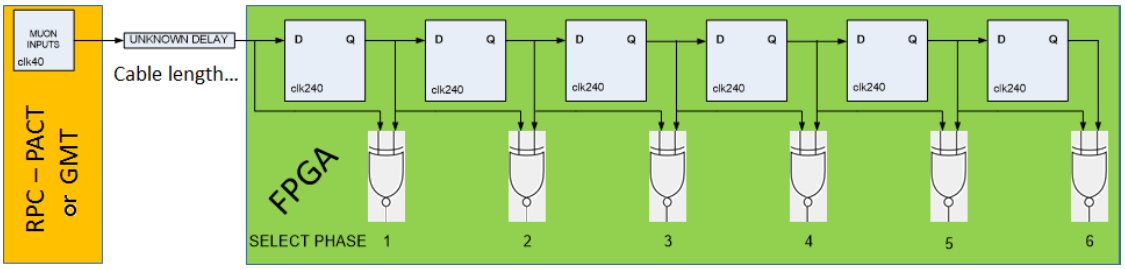


Figure 7.10: The receiver block that auto-chooses the optimum sampling phase

Low-rate receiver logic: Figure 7.10 gives the concept of the input logic, implemented to identify the optimum sampling point of the inputs signals and locks. Parallel patterns are sent every 25 ns (40 MHz) to the FPGA. The logic implements latches running six time faster (240 MHz). XNORs compare the inputs with the outputs in every latch and generate a GOOD flag. Then a FSM identifies the metastability location and forces the design to sample from the safe phase of the 40-MHz cycle. Figure 7.11, presents a snapshot of the input data locked to sample in the 3rd 40-MHz phase. The 64-bit input frame is capture correctly in the *muon_ output* signal (lower signal shown in the Figure).

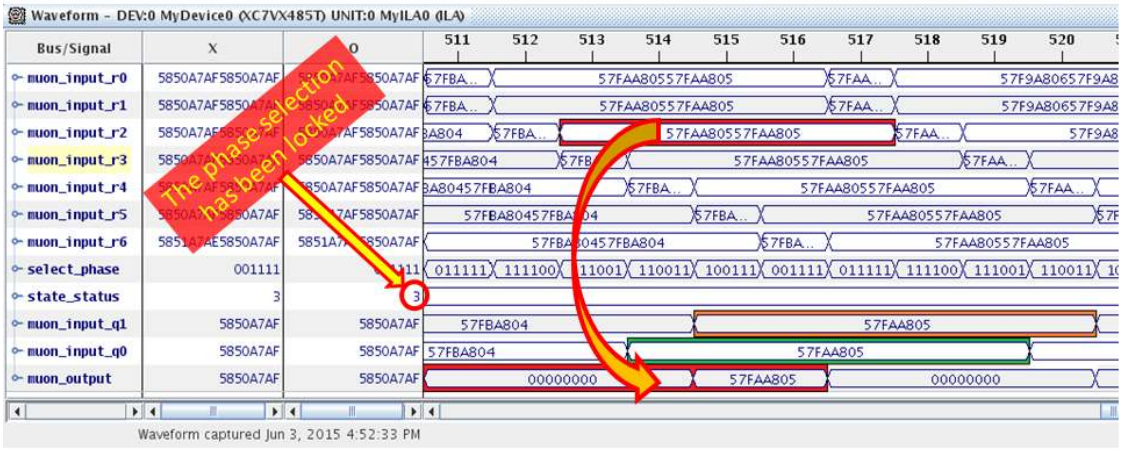


Figure 7.11: ISE Chipscope - Validation of the 40 Mb/s receiver block

Chapter 8

Summary and conclusions

CMS Level-1 muon Trigger Upgrade launched in the first quarter of 2016 was the result of a large collaboration working together in order to increase efficiency. The new L1T architecture has changed from detector-based scheme to a geometry-based system and the trigger redundancy has been moved earlier in the trigger chain. BMTF is the new regional muon trigger that is searching for muon tracks in the region $|\eta| < 0.83$.

This Thesis describes the work completed the L1T Upgrade. Most of the effort presented concerns firmware developing of the Barrel Muon Track Finder (BMTF) trigger subsystem. Chapter 7 and Appendix A present additional work: on developing of VHDL blocks shared among two data consentrators of the Level-1 muon Trigger chain and the Global Trigger (TwinMux, CPPF and AMC502) and on evaluating mezzanine cards used in the Timing Control and Distribution System (TCDS) in CMS L1T.

As luminosity and pile-up will be increased in CMS over the next years, higher trigger rates will be produced by the Trigger Primitives Generators (TPGs), requiring a more efficient and redundant L1T system with reduced trigger rate. For the central barrel trigger, the old Drift Tube Track Finder (DTTF) has been replaced by the Barrel Muon Track Finder. The new system follows the μTCA standard and is based on 12 Master Processor virtex-7 (MP7s), each hosting one FPGA large enough to implement track finder algorithms covering one barrel wedge.

The VHDL BMTF set of logic blocks uses IPbus interface between the processor and the control PC. Moreover it uses TCDS decoder and control, clock distribution via PLLs, several Finite State Machines, asynchronous 10-Gb/s protocol and readout block. The algorithm of the BMTF has been improved compared with the old DTTF. The new p_T resolution is increased using 9 bits (512 values) instead of 5 bits (32 values) used in DTTF. The p_T assignment is performed by the old (same implemented in DTTF) or the new algorithm. Both are running in parallel and the logic chooses one output of the two algorithms for each bunch crossing, depending on quality criteria. Latency has been significantly improved. BMTF spends 14 Bunch Crossings (BX) instead of 33 used by the DTTF. Firmware optimization keeps about 70% of the FPGA resources unused, reserved from future algorithm upgrades.

The design as well as the implementation of the BMTF have been validated with simulation tools as well as with injected muon patterns in the buffers of the cards. Python scripts injected 20,000 muon candidates, used as inputs of the MP7 cards. The output of the cards were compared against the emulator of the BMTF. During commissioning, and after thoroughly testing the setup, several firmware, hardware and software problems were fixed. Input and output data were collected through the DAQ network and the inputs were injected to a bit to bit C++ algorithm emulator. The output comparisons demonstrate an over-95% agreement between BMTF performance and emulator. The results of output comparisons indicate an agreement of data to emulator over than 95%. Efficiency plots show a plateau of BMTF over 90% (similar to DTTF) and trigger rate plots a 40% reduction compared to the legacy system which concludes that the BMTF is an improved track finder compared to DTTF.

The BMTF trigger subsystem is controlled by the common online software control, called SoftWare for Automating the conTrol of Common Hardware (SWATCH). In the firmware, control and status registers were implemented and connected to IPbus, with which the algorithm is configured according to the RUN conditions. Monitoring blocks count the trigger rate that appears in several stages of the algorithm and are monitored thought the SWATCH. Data Quality Monitoring (DQM) is used in order to provide a quick evaluation of the system while running.

VHDL blocks are re-designed in order to meet the requirements for the different FPGAs and shared among other L1T subsystems. Firmware is built for TwinMux, CPPF and AMC502 based on the BMTF logic blocks according to the corresponding project needs. The set of the logic blocks have been successfully tested.

VHDL projects have been designed in order to test FMC mezzanine cards and evaluate the PCB design. Those FMCs are used in the TCDS and distribute the LHC clock and TTC commands.

The work described on this Thesis, carried out according to the Technical Design Report: TDR2013 [1]. Four papers conserning the BMTF system, have been puplished, after work was presented in different conferences: TWEEP2015 [2], TWEEP2016 [3], ICHEP2016 [4] , VCI2016 [5]. One Detector Note [6] and one Twiki web-page [7] with useful instructions for the BMTF user have been provided by the Thesis's writer.

Appendix A

Evaluation of mezzanine cards used for the TCDS in CMS

Level-1 CMS Trigger upgrade intoduced in the contest of the old Timing and Trigger Control (TTC) has been replaced by the Trigger Control Distribution System (TCDS). The TCDS controls and synchronizes all trigger sub-systems and it is based in two μTCA boards: The AMC13 and the FC7 [55, 70, 71]. AMC13 is used as Central Partition Manager (CPM) and μTCA as readout board. FC7s is used as Local Partition Manager (LPM) and Partition Interface (PI). FC7 is a dual FMC carrier card capable to host two HPC-FMC mezzanines [72]. According to the mezzanines mounted in the FC7 and the corresponding firmware, it plays the role of LPM or PI. Figure A.1 shows the hardware used in LPM and PI systems. LPM-FC7 hosting the EDA-02708-V1 and the EDA-02707-V1. PI-FC7 hosting the EDA-02727-V1 and the EDA-02707-V1.

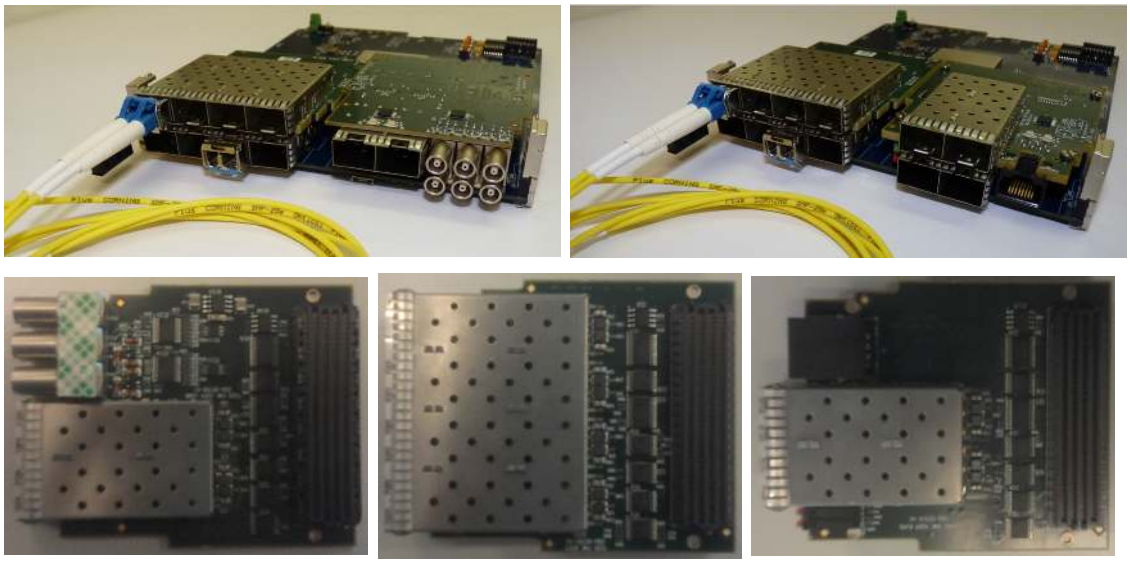


Figure A.1: Hardware used in the TCDS. Upper left: FC7 board as LPM, upper right: FC7 board as PI, down left: EDA-02708-V1 mezzanine, down middle: EDA-02707-V1 mezzanine, down right: EDA-02727-V1 mezzanine

CPM and LPM lie on the same μTCA crate and communicate via the backplane of the crate. LPM board receives L1As[27], BGo commands and LHC clock from the

CPM, it sends Trigger Throttle System (TTS) status to the CPM. In the front panel, LPM is equipped with high speed FMC EDA-02708-V1 running at 10 Gb/s and with 6 LEMO connectors. Both are used to send local trigger signals to the DAQ. The second mezzanine of the LPM (low speed FMC EDA-02707-V1), is used to transmit TTC commands to the PIs as well as to receive TTC status from PIs. PIs uses the low speed FMC EDA-02727-V1 in order to be interconnected with LPM.

A.1 FMC evaluation tests using the KC705 development board

The three FMCs mentioned previously have been evaluated using the KC705 platform. VHDL blocks has been developed in order to test loopback links running for several hours, validating a good performance of the tested mezzanines (EDA-02708-V1, 02707 EDA-02727-V1 and EDA-02727-V1) [73].

A.1.1 VHDL design for evaluating the PCB performance of EDA-02708-V1

The results taken after testing a commercial mezzanine card Faster Technology - F18, were used as reference to evaluate the output results of the EDA-02708-V1 testing, because both are high-speed cards hosting SFP+ optics, running up to 10 Gb/s [74]. Figure A.2 (left), shows the performance of the F18 card on the KC705 evaluation board and Figure A.2 (right), the EDA-02708-V1 card on the same board for the same test.

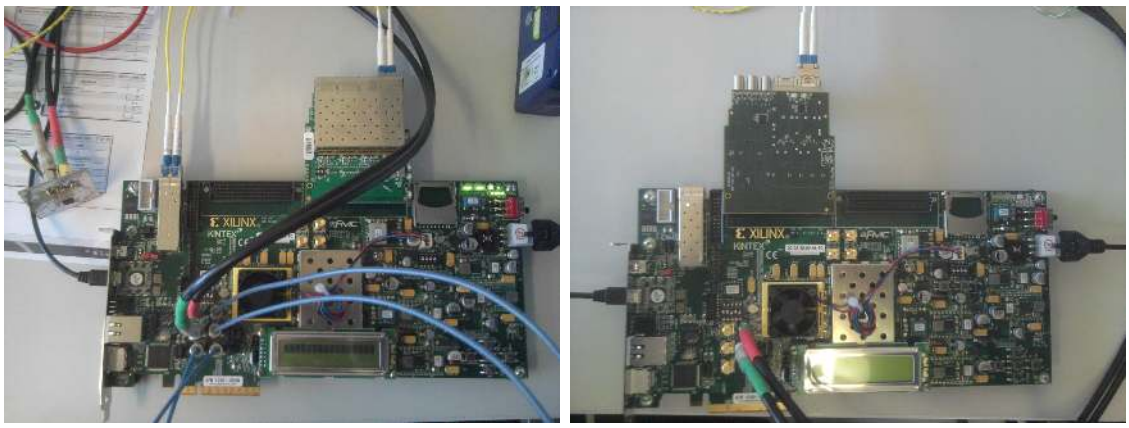


Figure A.2: KC705 used as the carrier platform testing the FMC cards. Left: Faster Technology F18 on KC705 platform, right: EDA-02708-V1 on KC705 platform.

The testing setup is shown in the right-hand side of Figure A.3. Both FMC tests were performed using the same equipment: evaluation board, SFP+ module, fiber, optical attenuator, optical splitter and power meter. In addition, the same firmware and the same Kintex transceiver channels were used. F18 mezzanine provides eight channels and EDA-02708-V1 two. The transceivers used for the test were X0Y12 and X0Y13 and belong to the BANK 118 of the *XC7K325T-2FFG900C* FPGA.

The test is based on the Xilinx IP integrated Bit Error Rate Test (iBERT). The implemented logic: it generates PRBS-7 data patterns, serializes the data, sends

them to the transmitting line, receives data from the input channel, deserializes the data to frames, checks if the frames belong to the PRBS-7 sequence and if not it increases an error counter. Moreover the logic uses: an I^2C interface to enable the SFPs though an I^2C switch, a state machine to control the I^2C and an MMCM to distribute the needed clocks. From the topology point of view (Figure A.3, right side) the SFP+ converts electrical signal to optical, the data stream passes through the attenuator, the optical signal splits into two and the 90% returns to the receiver of the FPGA while the 10% goes to a power meter for monitoring. The test measures the Bit Error Rates (BERs) as the attenuation increases and forms BERT curves.

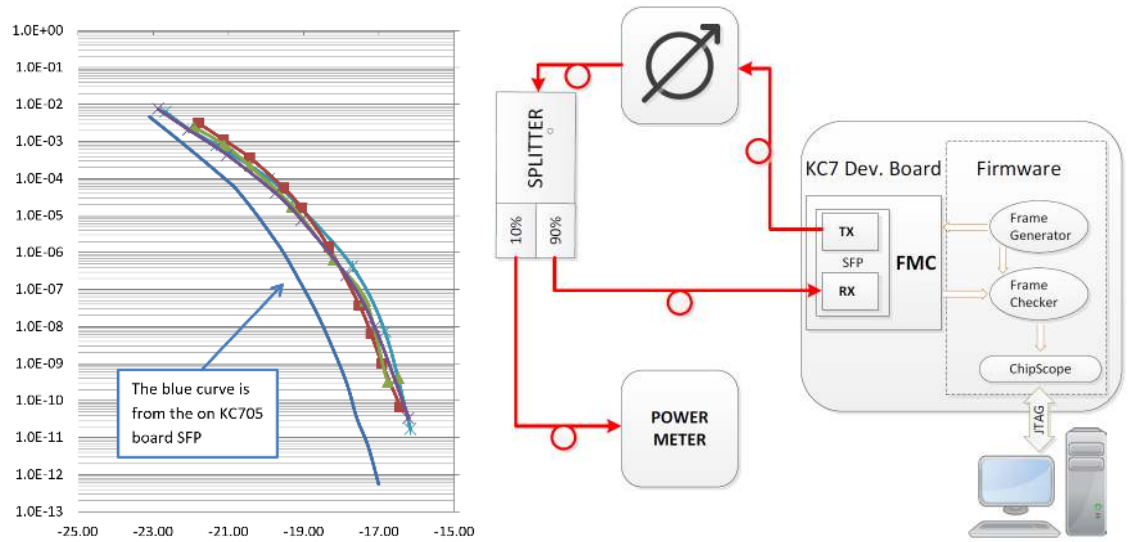


Figure A.3: Evaluation setup and BERT curves of F18 and EDA-02708-V1. Left: PCB performance - BERT curves. Y-axis represents the bit-error rate and X-axis the optical power in dbm. Right: Setup and logic for the evaluation test.

The test was performed on channel 0 (DP0) of F18 card. The results of the BER as well as the optical power were collected while the attenuation of the attenuator instrument was increased and light blue curve of Figure A.3 (left side) was formed. The test was repeated four more times: On channel 1 (DP1) of F18 (purple curve), on DP0 of EDA-02708-V1 (red curve), on DP1 of EDA-02708-V1 (green curve) and finally on the on-board SFP+ (dark blue curve). As it is shown, curves DP0, DP1 of F18 and EDA-02708-V1 are almost identical while the one on board is better. Therefore the EDA-02708-V1 card performs as well as the commercial specifications, a fact that demonstrates its good performance. In addition, as expected, the on-board transmission line gives a better BER curve since it has the best PCB trace compared with the mezzanine paths including the FMC connector.

A.2 VHDL design for evaluating the SERDES of EDA-02707-V1

Figure A.4 shows the EDA-02707-V1 mounted on the Xilinx board while testing. The EDA-02707-V1 mezzanine is designed to connect 8 SFPs to standard FPGA I/Os. The FPGA I/Os are accessible by FPGA SERDES. The SERDES are configurable hardware modules able to run in lower rates than the GTX or GTH transceivers.

The bandwidth of SERDES depended on the FPGA switching characteristics which in case of Xilinx 7 series FPGAs can not extend 1.6 Gb/s.

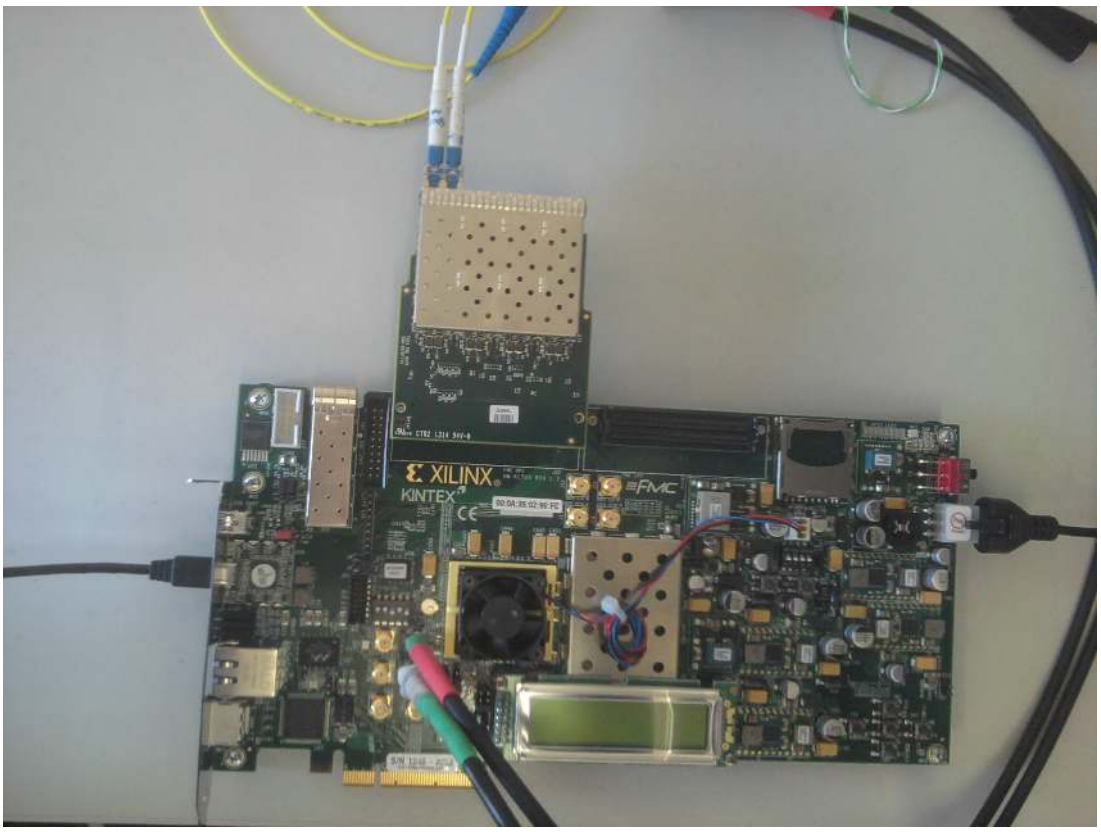


Figure A.4: EDA-02707-V1 on the KC705 platform

The block diagrams of the VHDL modules designed to evaluate EDA-02707-V1 is shown in Figure A.5. The top level of the VHDL contains:

- 2 MMCMs: to generate all needed clocks and shift the fast clock of the ISERDES in order to sample the received data correctly.
- 1 I^2C interface: to enable the SFPs modules via an I^2C switch.
- 1 common frame generator: simple counter.
- 1 common 8b/10b encoder: to achieve DC balance.
- 8 serializes: ratio 8:1.
- 8 deserializes: ratio 1:8.
- 8 8b/10b decoders: to decode the input data stream.
- 1 state machine: for bit slip.
- 1 synchronous demultiplexer: to control all ISERDES (FPGA fabric block).
- 8 error counters: to check for errors (one for each channel).

- 2 ILA (Indegraded Logic Analyser) cores: to illustrate signals (one for the common generator and one for the received frames).

Two different bandwidth tests were performed at 400 Mb/s and 800 Mb/s in calibrated channels. In both tests the attenuation was increased until the channel started to have errors. The initial calibration was done by forcing the frame generator to send zeros and shifting the phase of the ISERDES (receiver part) several times until the received frame became stable and then forced to bit slip until only zeros appeared to the input frames. Finally, the frame generator released and an error counter increased every time an error appears. Both tests were successful as there were running for several days without counting an error.

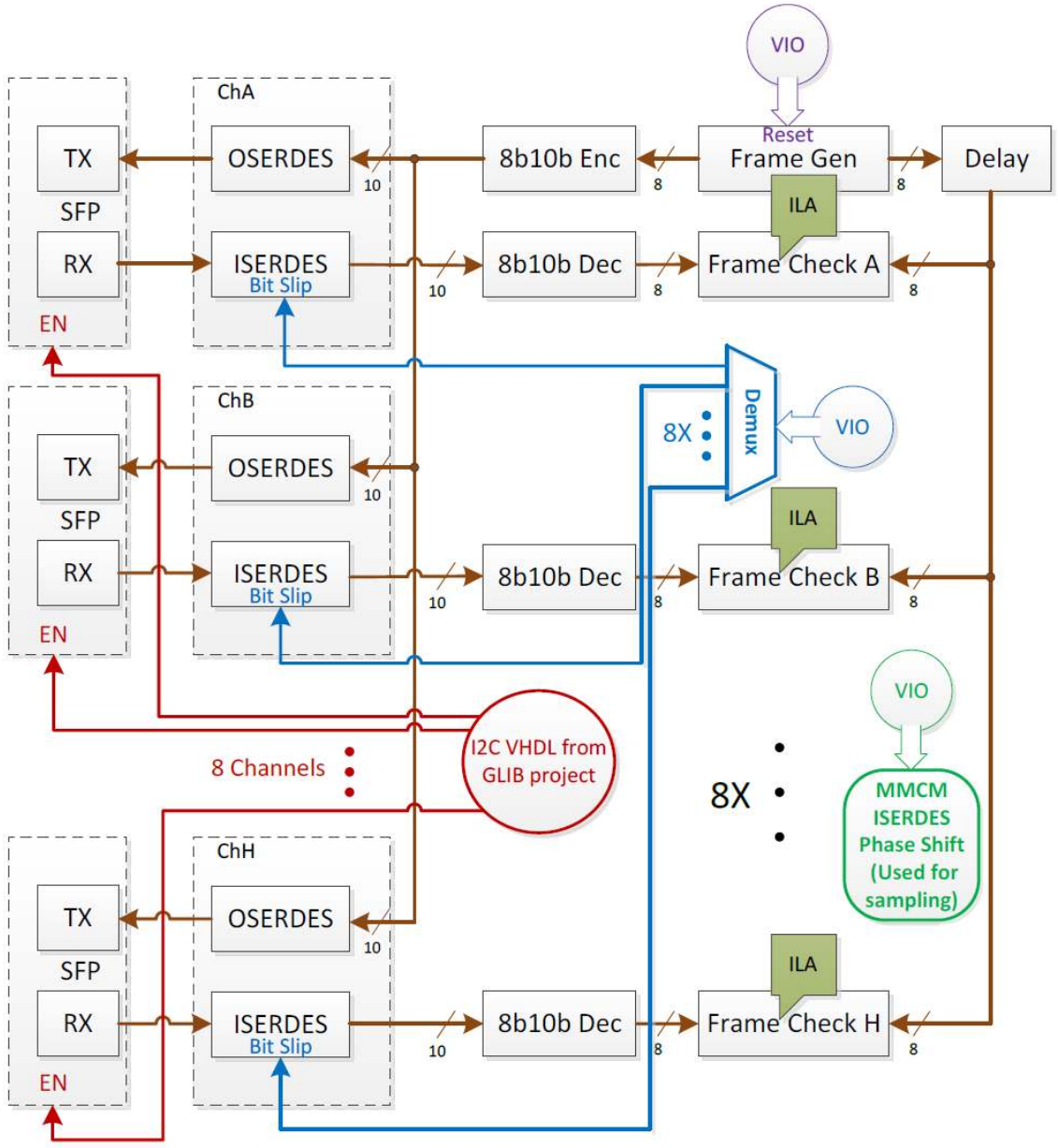


Figure A.5: VHDL block diagram used to evaluate EDA-02707-V1

In the previous setup an attenuator, a splitter and a power meter were added. The attenuation was increased until the point that the error counter started counting. In

both rates (400 or 800 Mb/s) and channels the attenuation limit was close to -20 dBm.

Figure A.6: Wide-open eye diagram at 400 Mb/s, indicating data transactions.

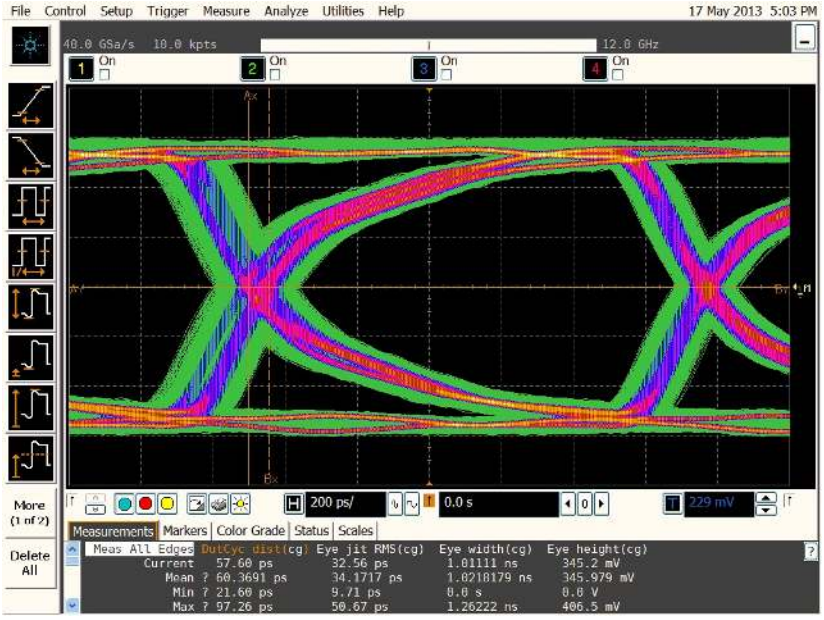


Figure A.7: Open eye diagram at 800 Mb/s, indicating safe data transactions.

Finally the test repeated for the 400 Mb/s and 800 Mb/s firmware version and the eye diagrams are shown in Figures A.6 and A.7. In these cases the output of the SFP channel H was driven to a digital analyzer. The occurred eyes are wide open, which indicates good transmission line of the PCB designed in the EDA-02707-V1 mezzanine card.

A.3 VHDL design for evaluating SPF and Ethernet links performance of EDA-02727-V1

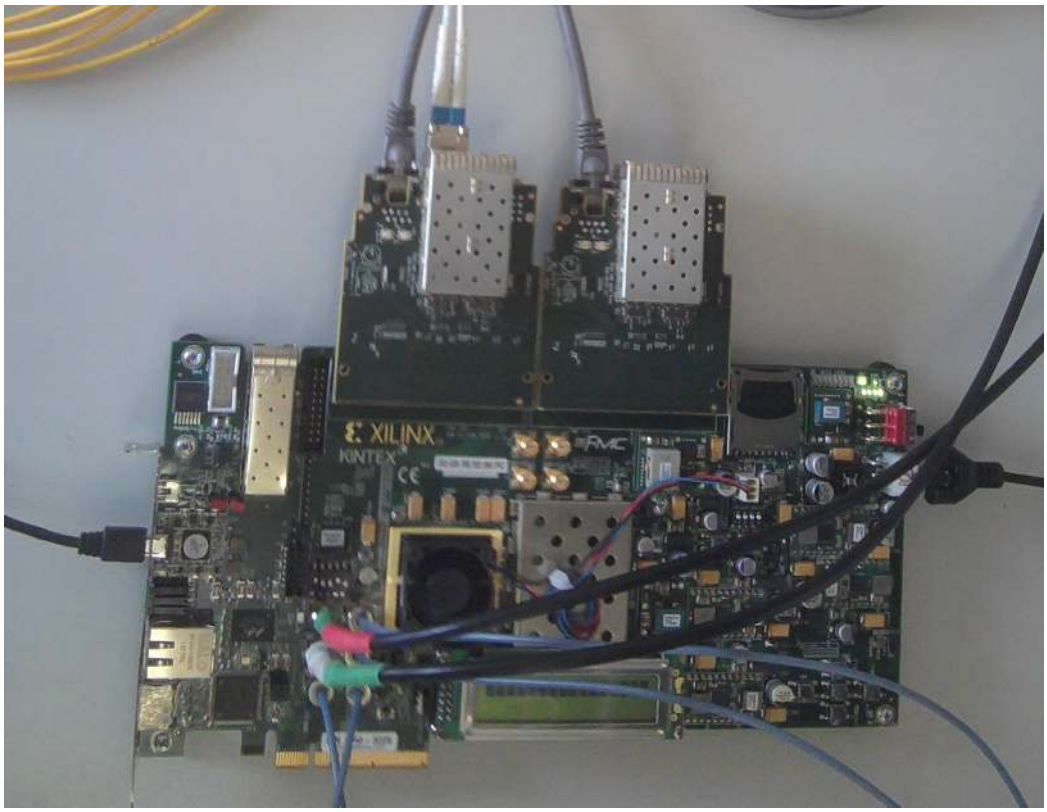


Figure A.8: Two EDA-02727-V1 mounted in the KC705 development card

EDA-02727-V1 card follows EDA-02707-V1 concept. Instead of 8 SFPs, the EDA-02727-V1 has 4 SFPs and the other 4 SERDES are connected to a RJ45 jack. Figure A.8 presents two EDA-02727-V1 FMCs mounted to the KC705 testing platform and interconnected with a not-cross over Ethernet cable. Figure A.9 shows the topology used for testing the Ethernet connection of this card. Since the signal is electrical there is no easy way to attenuate it. To evaluate the performance of those links the data loopbacked over the carrier FMCs for several hours and checked out the error counters.

The implemented logic is same as in the previous test:

- 2 MMCMs. In order to sample the received data stream the phase of the MMCM is changed dynamically.
- 1 I^2C interface to enable the SFPs.
- 1 common frame generator (simple counter).
- 1 common 8b/10b encoder.
- 8 serializes.
- 8 deserializes.

- 8 8b/10b decoders.
- 1 common 8b/10b encoder.
- 1 state machine for bit slip.
- 1 synchronous demultiplexer.
- 8 error counters (one for each channel).
- 2 Integrated Ligic Analyzer (ILA) cores to illustrate signals (one for the common generator and one for the received frames).

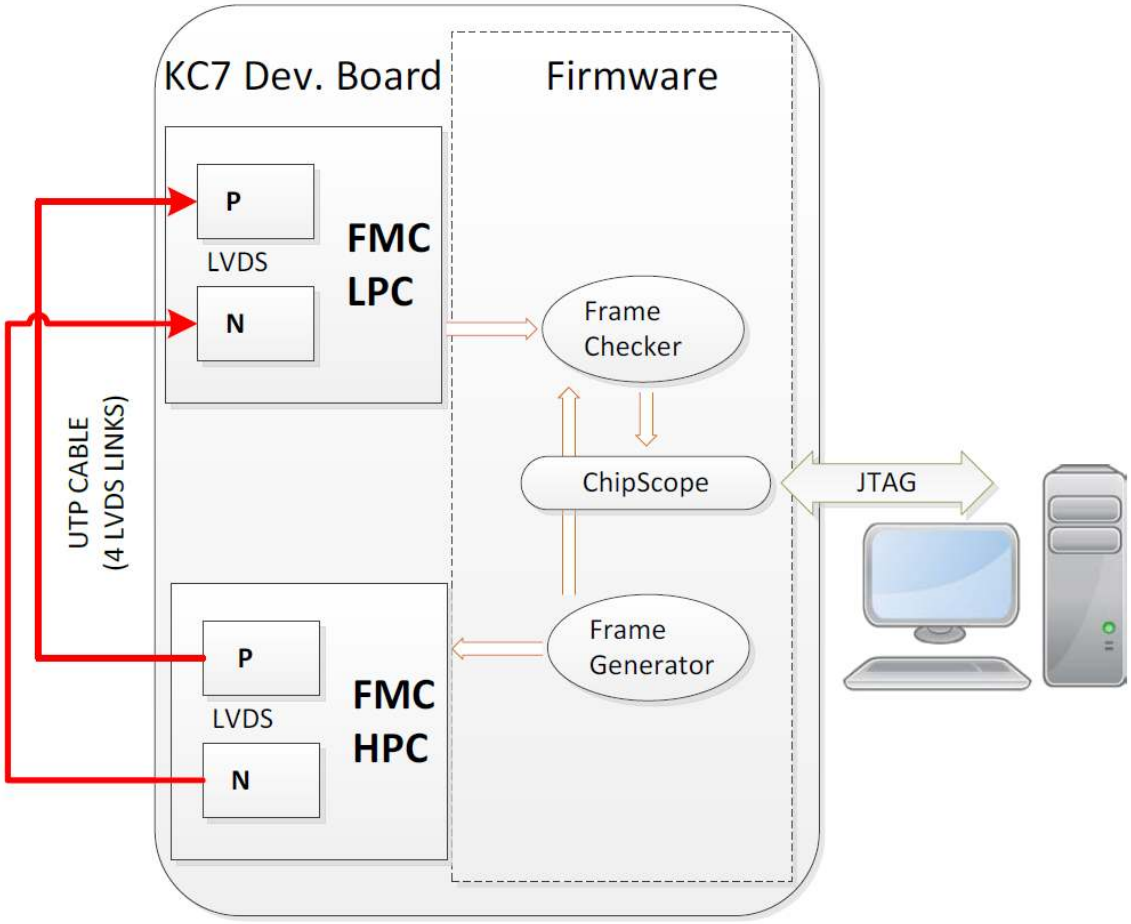


Figure A.9: Evaluation setup of copper links of EDA-02727-V1

Similar as in EDA-02707-V1 two different bandwidth tests have been performed. The fist at 400 Mb/s and the second at 800 Mb/s. In both cases the attenuation has been increased until the channel start to have errors. Calibration is also needed and it is mentioned in the previous Section. The attenuation limit is close to –20dBm. Channels E, F, G and H cannot be attenuated due to their nature (copper cable). After few days of continuously running no error occurred.

Appendix B

Input super-primitive format and channel mapping of the BMTF

This Appendix presents the input data format and the input channel mapping used to interconnect TwinMux and BMTF subsystems.

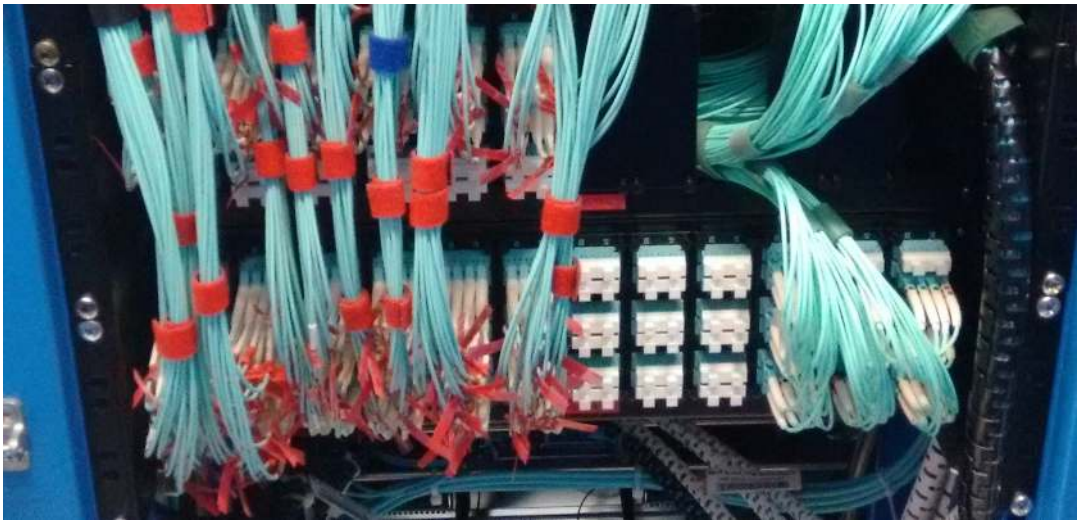


Figure B.1: Input BMTF fiber channels connected to the TwinMux patch panel

Each one of the 12 BMTF processor cards receives data from one track cable including 30 optical channels at 10 Gb/s. Each channel sends trigger primitives from one muon candidate and a pair of channels correspond to trigger primitives from on DT muon station. Every muon wedge has 5 sectors. Therefor each MP7 receives all muon primitives from one wedge and its neighbor.

B.1 Super-Primitive format

The channel pair is tagged as first (low) and second (high) channel. The primitive format (presented in Table B.1) consists of six 32-bit words. The first four have ϕ information, the fifth has the η of the hits and the sixth word is empty. The format of the first four words is identical. In particular, words 0, 1, 2 and 3, have data coming from the stations 1, 2, 3 and 4 (ST1, ST2, ST3 and ST4) and word 4 has the η information of eta stations 1, 2 and 3.

0	BC	NC	C	R	S	QL	PhiB	Phi	
	31	29	27	26	25	24	21	11	0
1	BC	NC	C	R	S	QL	PhiB	Phi	
	31	29	27	26	25	24	21	11	0
2	BC	NC	C	R	S	QL	PhiB	Phi	
	31	29	27	26	25	24	21	11	0
3	BC	NC	C	R	S	QL	PhiB	Phi	
	31	29	27	26	25	24	21	11	0
4	BC	NC					HitsSt3	HitsSt2	HitsSt1
	31	29					20	13	6 0
5	BC	NC							
	31	29							0

Table B.1: Muon data sent over in one bunch-crossing. Each row shows one 32-bit word. The data of the six rows are the super-primitives.

The two most significant bits of every word are the two list significant bits of the Bunch Counter (BC) sending by the TwinMux. Since the bunch counter changes every 25 ns and the input segments are synchronized, all BC should have the same value for six 32-bit words and change once every time a new 1st word appears. The list below explains all Acronyms of the Table B.1.

- Words 0, 1, 2 and 3: Data from the corresponding ϕ stations.
  - **BC**: *2-bits*. Two Least Significant Bits (LSBs) of the bunch counter.
  - **NC**: *2-bits*. Reserved.
  - **C**: *1-bit*. Calibration bit from the minicrate. Not used.
  - **R**: *1-bit*. '1' indicates RPC presence. Only used in monitoring blocks.
  - **S**: *1-bit*. '1' indicates Super-primitive presence (DT + RPC) and '0' primitive presence (only DT).
  - **QL**: *3-bits*. DT quality bits. "111" indicates null; "000", "001" and "010" uncorrelated DT measurement; "011", "100", "101" and "110" correlated DT measurement. $0 -> 6$: Lower to higher quality.
  - **PhiB**: *10-bits*. Bending primitive in ϕ. 2's complement with range from -512 to 511.
  - **Phi**: *12-bits*. ϕ coordinate primitive (muon stab). 2's complement with range from -2,048 to 2,047.
- Words 4: Data from η stations.
  - **BC, NC**: *2-bits, 9-bits*. As in words 0 to 3.
  - **HitsSt3**: *7-bits*. η quality bits or[1] hits of station 3. '1'=true, '0'=false.
  - **HitsSt2**: *7-bits*. η quality bits or[1] hits of station 2. '1'=true, '0'=false.
  - **HitsSt1**: *7-bits*. η quality bits or[1] hits of station 1. '1'=true, '0'=false.

[1]The channel 1 (low) of the pair of channels per station contain the η quality bits and the 2nd channel (high) the η hit bits.

- Words 5: Empty word.
  - **BC, NC**: *2-bits, 30-bits.* As in words 0 to 3.

B.2 Interconnections

The labels written in red tags of the LC connectors (shown in the Figure B.1) are listed in the table B.2. The table mapping shows the input connections of BMTF for the wedge n, where n∈[1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12]. The first column gives the wheel number of the input channel, the second the LC connector number, the third the VHDL channel number, the forth the channel input, the fifth the algorithm input name and the sixth shows comments, concerning the location of the mapping.

Wheel	LC number	LC Label	Channel input	Algo Inputs	LC channel description
-2	1	$Wn2S(n-1)M1$	0	*dn2wlsl*	-2 Wheel,left Sector,1st (low)
-2	2	$Wn2S(n-1)M2$	1	*dn2wlsh*	-2 Wheel,left Sector,2st (high)
-2	3	$Wn2S(n+1)M2$	2	*dn2wrsl*	-2 Wheel,right Sector,1st (low)
-2	4	$Wn2S(n+1)M2$	3	*dn2wrsh*	-2 Wheel,right Sector,2st (high)
-2	5	$Wn2S(n)M1$	4	*dn2wosl*	-2 Wheel,own Sector,1st (low)
-2	6	$Wn2S(n)M2$	5	*dn2wosh*	-2 Wheel,own Sector,2st (high)
-1	9	$Wn1S(n-1)M1$	8	*dn1wlsl*	-1 Wheel,left Sector,1st (low)
-1	10	$Wn1S(n-1)M2$	9	*dn1wlsh*	-1 Wheel,left Sector,2st (high)
-1	11	$Wn1S(n+1)M2$	10	*dn1wrsl*	-1 Wheel,right Sector,1st (low)
-1	12	$Wn1S(n+1)M2$	11	*dn1wrsh*	-1 Wheel,right Sector,2st (high)
-1	13	$Wn1S(n)M1$	12	*dn1wosl*	-1 Wheel,own Sector,1st (low)
-1	14	$Wn1S(n)M2$	13	*dn1wosh*	-1 Wheel,own Sector,2st (high)
0	17	$W0S(n-1)M1$	16	*d0wlsl*	0 Wheel,left Sector,1st (low)
0	18	$W0S(n-1)M2$	17	*d0wlsh*	0 Wheel,left Sector,2st (high)
0	19	$W0S(n+1)M2$	18	*d0wrsl*	0 Wheel,right Sector,1st (low)
0	20	$W0S(n+1)M2$	19	*d0wrsh*	0 Wheel,right Sector,2st (high)
0	21	$W0S(n)M1$	20	*d0wosl*	0 Wheel,own Sector,1st (low)
0	22	$W0S(n)M2$	21	*d0wosh*	0 Wheel,own Sector,2st (high)
+1	23	$Wp1S(n)M1$	22	*dp1wosl*	+1 Wheel,own Sector,1st (low)
+1	24	$Wp1S(n)M2$	23	*dp1wosh*	+1 Wheel,own Sector,2st (high)
+1	25	$Wp1S(n-1)M2$	24	*dp1wlsl*	+1 Wheel,left Sector,1st (low)
+1	26	$Wp1S(n-1)M2$	25	*dp1wlsh*	+1 Wheel,left Sector,2st (high)
+1	27	$Wp1S(n+1)M1$	26	*dp1wrsl*	+1 Wheel,right Sector,1st (low)
+1	28	$Wp1S(n+1)M2$	27	*dp1wrsh*	+1 Wheel,right Sector,2st (high)
+2	29	$Wp2S(n)M1$	28	*dp2wosl*	+2 Wheel,own Sector,1st (low)
+2	30	$Wp2S(n)M2$	29	*dp2wosh*	+2 Wheel,own Sector,2st (high)
+2	33	$Wp2S(n-1)M2$	32	*dp2wlsl*	+2 Wheel,left Sector,1st (low)
+2	34	$Wp2S(n-1)M2$	33	*dp2wlsh*	+2 Wheel,left Sector,2st (high)
+2	35	$Wp2S(n+1)M1$	34	*dp2wrsl*	+2 Wheel,right Sector,1st (low)
+2	36	$Wp2S(n+1)M2$	35	*dp2wrsh*	+2 Wheel,right Sector,2st (high)

Table B.2: TwinMux to BMTF channel mapping. n represents the wedge number

Appendix C

Output bits and scales of the BMTF system

Every BMTF card sends 3 muon canditates per bunch crossing to μGMT using one optical channel 61 (firmware output 61). Also it duplicates the same output to channel 60 as a fiber fallback option.

Figure C.1: Output BMTF fiber channels connected to the BMTF cards

C.1 BMTF output data format

0	*X0*	ϕ			*F*	η			*Qual*	p_T	
	31	30			22	21			12	8	0
1	*SE*	*NA*	*NC*		*WN*	*NC*	*Track Addresses*		*NC*	*VC*	*CH*
	31	30	29		22	19	17		3	1	0
2	*B0*	ϕ			*F*	η			*Qual*	p_T	
	31	30			22	21			12	8	0
3	*B1*	*NA*	*NC*		*WN*	*NC*	*Track Addresses*		*NC*	*VC*	*CH*
	31	30	29		22	19	17		3	1	0
4	*B2*	ϕ			*F*	η			*Qual*	p_T	
	31	30			22	21			12	8	0
5	*NC'*	*NA*	*NC*		*WN*	*NC*	*Track Addresses*		*NC*	*VC*	*CH*
	31	30	29		22	19	17		3	1	0

Table C.1: Muon data are sent over during one bunch-crossing, each row shows one 32-bit word, thus, two rows represent one muon.

The three muon candidates are encoded using 64 bits and thus send in six 32-bit words over two 240-MHz clock cycles (Table C.1).

- 30 Least Significant Bits, words 0, 2 and 4: Physical parameters of 1st, 2nd and 3rd found muons.
  - p_T: 9 bits. Transverse momentum, hardware value.
  - *Qual*: 4 bits. Express the track quality.
  - η: 9 bits eta (pseudorapidity).
  - F: 1 bit. Fine-eta bit.
  - ϕ: 8 bits. Azimuth angle.
- 30 Least Significant Bits, words 1, 3 and 5: Track identification of 1st, 2nd and 3rd found muons.
  - *CH*: 1 bit. Indicates -1^n charge when CH is n.
  - *VC*: 1 bit. 1: Indicates CH bit is valid and 0: is not valid.
  - *Track Addresses*: 14 bits. Determines the track segments used to construct the muon track.
  - *WN*: 3 bits. Indicates the wheel of the found muon.
  - *NA*: 1 bit. 1: Indicates the new algorithm (Subsection 4.1.2.3) was used to find the muon and 0: the old algorithm was used.
- Most Significant Bit of all words
  - *X0*: Bunch crossing zero bit. 1: bunch crossing zero of orbit; 0: else.
  - *SE*: Synchronization error. 1: error; 0: no error.
  - *B2, B1, B0*: 3 Less Significant Bits of the bunch crossing counter.
  - *NC*: Reserved.

C.2 Encoding and scales

Scales for η, ϕ and p_T are linear. In contrast the fine bit (F) as well as the *Track Addresses* contain information about the muon track. The 4 quality bits are split into two parts where the two Most Significant Bits are “00” when no muon track found and “11” otherwise. The two Least Significant Bits categorize the muon track quality.

The following coordinate system is used for the η and ϕ coordinates:

- CMS is north of centre of LHC; right handed system with origin in collision point.
- Horizontal x-axis pointing to centre of LHC (south).
- Vertical y-axis pointing upwards.
- Horizontal z-axis horizontal pointing to west, parallel to beam, parallel to B-field.

- Global $\phi = 0°$ corresponding to x-axis, $\phi = 90°$ corresponding to y axis. The track-finder systems transmit relative ϕ coorindates where $\phi = 0°$ lines up with the lower sector or wedge boundary of the individual processor. For details, see Section C.2.1.
- $\eta = 0$ in x-y plane, $\eta > 0$ for positive z-axis.

Parameter	n_{bits}	Unit/step u	Range	Comment
p_T	9	0.5 GeV	$0 \rightarrow 511$	0: empty candidate; $(bit\_value - 1) \times u$ p_T is defined at 90% efficiency as in the old trigger.
Quality	4			The two Most Significant Bits (MSB): "00" indicates no track and "11" valid track. The two LSB: categories the muon track according to a quality tag. (section C.2.7).
η	9	0.010875	-230 $\rightarrow$ 230	2's complement. $bit\_value \times u$ step gives the centre of the bin.
Fine bit	1			Indicates η-fine bit.
ϕ_l	8	$2\pi/576$	Sec. C.2.1	2's complement. $bit\_value \times u$ gives the lower edge of the bin.
Charge sign	1			1: negative, 0: positive
Valid charge	1			1: charge sign is valid, 0: charge sign cannot be determined
Track Address	14			see Sec. C.2.6
WN	3		Sec. C.2.8	Wheel of the muon
NA	1			New algorithm flag
X0	1			BC zero bit per link
SE	1			Synchronization error per link
BX0	3			3 Least Significant Bits of the bunch crossing counter. Per link.

Table C.2: Scale definitions of muon candidates of the BMTF output.

C.2.1 PHI scale

The BMTF transmits the muon's local phi value (ϕ_l) with a relative coordinate in a 8-bit scale, encoded in 2's complement and with the stepsize of $2\pi/576$. The μGMT (next step in the trigger chain), applies offsets to calculate the global ϕ coordinate that corresponds to the standard CMS coordinate system. Figure C.2 shows the global coordinate system in conjunction with the coordinate systems that apply for the track finders. Two conventions are necessary as the BMTF processors take one DT wedge of 30° into account, while the EMTF and OMTF use the 60° sectors of the CSC system. In both cases, the lower boundary of the wedge / sector corresponds to $\phi_l = 0°$.

- The BMTF transmits a signed value encoded in 2's complement. The range expected is -8 to 56 (corresponding to -5° to 35°), where the first and last 8 values (corresponding to 5° each) are overlapping with the previous and next processor.
- The EMTF and OMTF also transmit a signed value encoded in 2's complement. The expected range is -16 to 100 (corresponding to -10° to 62.5°), where the

first 16 and last 4 values (corresponding to 10° and 2.5° respectively) are overlapping with the previous and next processor.

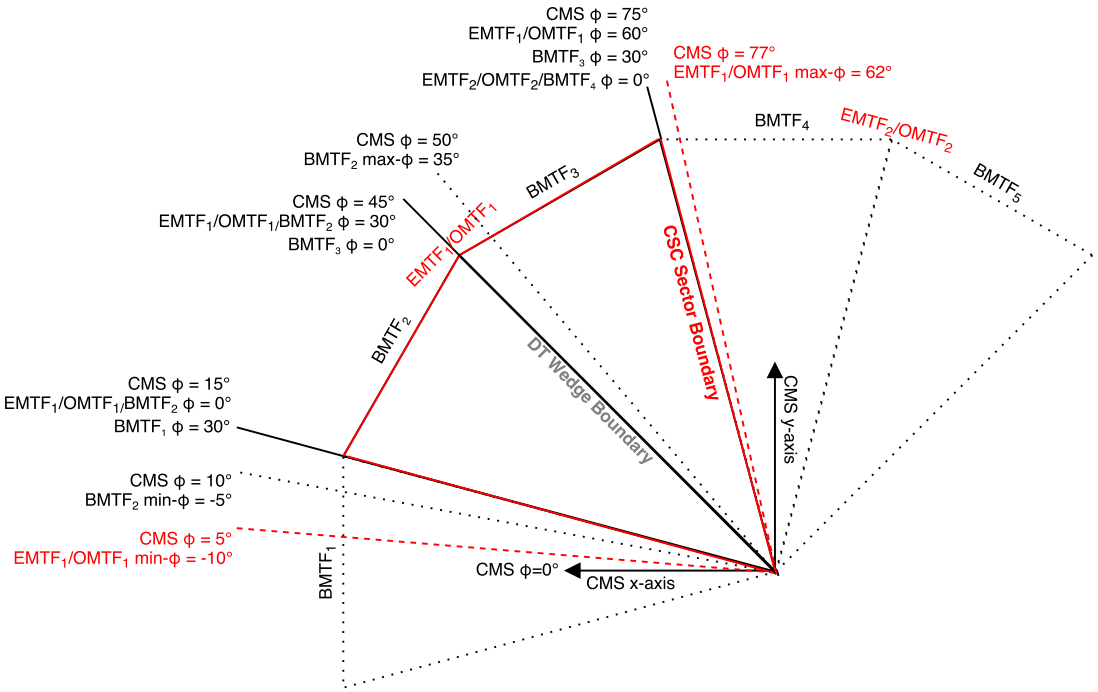


Figure C.2: Relative ϕ-scale for the track finders starts counting at the edge of the processed wedge or sector. The range is different for BMTF as it processes 30° wedges, and OMTF/EMTF which process the 60° sectors.

C.2.2 ETA scale

Instead of using θ angle[1], the BMTF expressed this coordinate in η pseudorapidity[2] which in CMS scale is linear. η is encoded using two's complement in 9 bits with a range from -230 to 230 in steps of 0.010875. η is marked by the *Fine bit (F)*.

C.2.3 Fine bit

The Fine bit (F) is used to encode whether the η coordinate could be determined precisely (F = 1) or not (F = 0).

C.2.4 p_T scale

The p_T scale is linear. It is encoded as an unsigned integer of 9 bits with a step-size of 0.5 GeV. The range is 3 to 140 GeV. A value of 0 indicates an empty candidate.

[1]The angle between the trajectory of the particle and the beam axis.
[2]Pseudorapidity equation: $\eta = -ln[\tan\frac{\theta}{2}]$.

C.2.5 Charge and charge valid bit

The valid charge bit (VCH) signifies validity of an assigned charge. The charge bit is 0 for positive charge and 1 for negative charge (charge = $(-1)^{sign}$).

C.2.6 Track addresses

The track addresses are encoded in 14 bits which is a concatenation of 2-4-4-4 bits representing stations addresses TS1, TS2, TS3 and TS4. Table C.3 shows all the values station addresses which the 14-bit Track Address can take. The address assignment is described further in Subsection 4.1.2.2.

	Left wedge			**Own wedge**			**Right wedge**		
	TS1	TS2	Null	TS1	TS2	Null	TS1	TS2	Null
Wheel n+1	2	3	F	0	1	F	4	5	F
Wheel n	A	B	F	8(2*)	9(1*)	F(3*)	C	D	F

Table C.3: BMTF Track Addresses

* Those track address are referred to TS1 station.

C.2.7 Quality scale

The quality of a muon track is encoded in 4 bits that are split into half. Two Most Significant Bits (MSB): "00" indicate no track and "11" found track. The two Least Significant Bits (LSB) categorize the track quality according to the muon stations (TS1, TS2, TS3 and TS4) tagging the track:

- "11" indicates track tagged for all four stations: TS1 → TS2 → TS3 → TS4.
- "10" indicates track tagged for three stations: TS1 → TS2 → TS3 or TS1 → TS2 → TS4 or TS1 → TS3 → TS4 or TS2 → TS3 → TS4.
- "01" indicates track tagged for two stations starting from the 1st: TS1 → TS2 or TS1 → TS3 or TS1 → TS4.
- "00" indicates track tagged for two stations: TS2 → TS3 or TS2 → TS4 or TS3 → TS4.

Hence the lower to higher quality track categories are: 0x0, 0xc, 0xd, 0xe and 0xf.

C.2.8 Wheel number

The wheel number bits are split in the Most Significant Bit (MSB) which indicates the sign and the other two bits indicating the number. Table C.4 shows the encoding.

Wheel name	**Encoding bits**	
	sign	number
-2	'1'	"10"
-1	'1'	"01"
-0	'1'	"00"
+0	'0'	"00"
+1	'0'	"01"
+2	'0'	"10"

Table C.4: Wheel number encoding

Appendix D

Access the BMTF hardware at CMS and execute basic tests

BMTF cards are accessible by the CMS control room through SWATCH [75]. Alternative access to the BMTF system requires a connection to the CMS network or requires the establishment of a tunnel connection to it. All MP7 as well as the single width AMCs (MCH and AMC13) cards are accessible though their MAC addresses.

D.1 BMTF Hardware Access

Information about the BMTF MAC addresses can be found in the BMTF collaboration web page [7]. In the same Twiki the user can find up to the latest BMTF design and the corresponding firmware binfiles. The BMTF Boards are accessed from the PC **srv-s2g16-34-01.cms** through the bridge PC **ctrl-s2c16-17-01.cms**. The tables below give the MAC addresses and the alias for each one of the AMCs for both BMTF crates.

	MAC	ALIAS
AMC13-kintex	08:00:30:f3:01:4a	amc-s1d03-17-13-t1
AMC13-spartan	08:00:30:f3:01:0a	amc-s1d03-17-13-t2
MCH	00:40:42:0b:1d:a6	mch-s1d03-17-01

Table D.1: Single width AMCs of the TOP BMTF crate. The AMC13 is connected to the FED 1376 and has two FPGAs (Kintex-7 and Spartan-6).

WEDGE	01	02	03	04	05	06
SLOT (XX)	01	03	05	07	09	11
MAC (YY)	98	bf	b3	c3	b4	ad

Table D.2: The double width AMCs of the TOP BMTF crate are the wedge processors: MP7s 1, 2, 3, 4, 5 and 6. WEDGE defines MP7 wedge processor. Each MP7 has the MAC 08:00:30:f3:03:YY and the alias amc-s1d03-17-XX, where YY and XX are defined as MAC and SLOT.

	MAC	ALIAS
AMC13-kintex	08:00:30:f3:01:de	amc-s1d03-09-13-t1
AMC13-spartan	08:00:30:f3:01:9e	amc-s1d03-09-13-t2
MCH	00:40:42:0b:1d:b8	mch-s1d03-09-01

Table D.3: Single width AMCs of the BOTTOM BMTF crate. The AMC13 is connected to the FED 1377 and has two FPGAs (Kintex-7 and Spartan-6).

WEDGE	07	08	09	10	11	12
SLOT (XX)	02	04	06	08	10	12
MAC (YY)	b7	a5	b2	a7	aa	c4

Table D.4: The double width AMCs of the BOTTOM BMTF crate are the wedge processors: MP7s 1, 2, 3, 4, 5 and 6. WEDGE defines MP7 wedge processor. Each MP7 has the MAC 08:00:30:f3:03:YY and the alias amc-s1d03-17-XX, where YY and XX are defined as MAC and SLOT.

D.2 Basic Tests

All systems based on the MP7 platform in CMS L1 Trigger Upgrade are controlled through uhal [76] libraries written in C++ and controld by C++ or python scripts. Simple IP connection, links alignment, channel loopbacks and more tests mast executed from the user in case of a setup intervention like a change of a card or a serious system failure. Commands of the mp7butler script which is available for check-out in cactus svn server following the MP7 software news web page [77]. Also BMTF scripts capable to configure the BMTF algorithms can be found in the BMTF cactus trunk [78]. Below is a list of commands that perform basic functions to test the BMTF system after intervention.

```
#To check out the IP connection to the bmtf_w1 MP7.
mp7butler.py connect bmtf_w12

#To print the BMTF firmware version of bmtf_w1.
mp7butler.py inspect bmtf_w1 infra

#To reset the MP7 processor of the 12th wedge.
mp7butler.py reset bmtf_w12

#To check the links alignment of processor $1 on the channels $2.
mp7butler.py rxalign bmtf_w$1 -e $2

#To set the $1 MP7 buffers to capture mode.
mp7butler.py buffers bmtf_w$1 captureRxTx

#To capture the $2 channels of MP7 $1 card.
mp7butler.py capture bmtf_w$1 -e $2

#To configure the BMTF algorithm of the $1 card.
Regs_read_7-11.py $1
```

```
#To Monitor the trigger rates of the BMTF card $1.
Moni_read_7-11.py $1
```

To connect the MP7 cards, the user has to use the XML address table stored in the *BMTF cactus address table*. This XML is referred as *bmtf_xe_220/mp7_payload.xml* in the framework address table shown below:

```
<?xml version="1.0" encoding="UTF-8"?>
  <connection id="bmtf_w1" uri="chtcp-2.0://ctrl-s2c16-17-01:10203?
   target=amc-s1d03-17-01:50001"address_table="file://
   ${MP7_ETC}/mp7/addrtab/bmtf_xe_220/mp7xe_infra.xml"/>
  <connection id="bmtf_w2" uri="chtcp-2.0://ctrl-s2c16-17-01:10203?
   target=amc-s1d03-17-03:50001" address_table="file://
   ${MP7_ETC}/mp7/addrtab/bmtf_xe_220/mp7xe_infra.xml"/>
  <connection id="bmtf_w3" uri="chtcp-2.0://ctrl-s2c16-17-01:10203?
   target=amc-s1d03-17-05:50001" address_table="file://
   ${MP7_ETC}/mp7/addrtab/bmtf_xe_220/mp7xe_infra.xml"/>
  <connection id="bmtf_w4" uri="chtcp-2.0://ctrl-s2c16-17-01:10203?
   target=amc-s1d03-17-07:50001" address_table="file://
   ${MP7_ETC}/mp7/addrtab/bmtf_xe_220/mp7xe_infra.xml"/>
  <connection id="bmtf_w5" uri="chtcp-2.0://ctrl-s2c16-17-01:10203?
   target=amc-s1d03-17-09:50001" address_table="file://
   ${MP7_ETC}/mp7/addrtab/bmtf_xe_220/mp7xe_infra.xml"/>
  <connection id="bmtf_w6" uri="chtcp-2.0://ctrl-s2c16-17-01:10203?
   target=amc-s1d03-17-11:50001" address_table="file://
   ${MP7_ETC}/mp7/addrtab/bmtf_xe_220/mp7xe_infra.xml"/>
  <connection id="bmtf_w7" uri="chtcp-2.0://ctrl-s2c16-17-01:10203?
   target=amc-s1d03-09-02:50001" address_table="file://
   ${MP7_ETC}/mp7/addrtab/bmtf_xe_220/mp7xe_infra.xml"/>
  <connection id="bmtf_w8" uri="chtcp-2.0://ctrl-s2c16-17-01:10203?
   target=amc-s1d03-09-04:50001" address_table="file://
   ${MP7_ETC}/mp7/addrtab/bmtf_xe_220/mp7xe_infra.xml"/>
  <connection id="bmtf_w9" uri="chtcp-2.0://ctrl-s2c16-17-01:10203?
   target=amc-s1d03-09-06:50001" address_table="file://
   ${MP7_ETC}/mp7/addrtab/bmtf_xe_220/mp7xe_infra.xml"/>
  <connection id="bmtf_w10" uri="chtcp-2.0://ctrl-s2c16-17-01:10203?
   target=amc-s1d03-09-08:50001" address_table="file://
   ${MP7_ETC}/mp7/addrtab/bmtf_xe_220/mp7xe_infra.xml"/>
  <connection id="bmtf_w11" uri="chtcp-2.0://ctrl-s2c16-17-01:10203?
   target=amc-s1d03-09-10:50001" address_table="file://
   ${MP7_ETC}/mp7/addrtab/bmtf_xe_220/mp7xe_infra.xml"/>
  <connection id="bmtf_w12" uri="chtcp-2.0://ctrl-s2c16-17-01:10203?
   target=amc-s1d03-09-12:50001" address_table="file://
   ${MP7_ETC}/mp7/addrtab/bmtf_xe_220/mp7xe_infra.xml"/>
</connections>
```

Appendix E

VHDL code used in BMTF

BMTF firmware has been designed in VHDL Hardware Description Language. BMTF contains more than 50,000 VHDL and Tcl code lines distributed in more than 100 files. On this Appendix few parts of those files are shown.

E.1 MP7 top file

The MP7 top file contains all basic instances of the system:

- **mp7xe infra:** Provides the basic infrastructure of the system. The instance implements a parallel interface to the microcontroller, an I^2C interface for the Xpoint switches and the jitter cleaner chips, SPI interfaces for the minipod optics, IPbus core logic and the clock generators.
- **mp7 ctrl:** Controls the main BMTF functions (configure, reset ...)
- **mp7 ttc:** Time and Trigger Control (TTC) logic, includes a ttc receiver and decoder, provides running signals such as the first bunch crossing of the beam orbit (BC0) and Level-1 Accept (L1A) and controls start - stop running modes.
- **mp7 datapath:** Implements 10-Gb/s serial link as well as the multi-functional channel buffers.
- **mp7 readout:** Which implements the logic that concentrates the event data which are send to the AMC13 board of the crate when L1A arrives in the BMTF as well as function utilities in order to suppress empty events.

```
library ieee;
use ieee.STD_LOGIC_1164.ALL;

use work.ipbus.all;
use work.ipbus_trans_decl.all;
use work.mp7_data_types.all;
use work.mp7_readout_decl.all;
use work.mp7_ttc_decl.all;
use work.mp7_brd_decl.all;
```

```
library UNISIM;
use UNISIM.VComponents.all;

entity top is
   port(
      eth_clkp, eth_clkn: in std_logic;
      eth_txp, eth_txn: out std_logic;
      eth_rxp, eth_rxn: in std_logic;
      leds: out std_logic_vector(11 downto 0);
      ebi_nwe: in std_logic;
      ebi_nrd: in std_logic;
      ebi_d: inout std_logic_vector(15 downto 0);
      ebi_a: inout std_logic_vector(16 downto 1);
      clk40_in_p: in std_logic;
      clk40_in_n: in std_logic;
      ttc_in_p: in std_logic;
      ttc_in_n: in std_logic;
      clk_cntrl: out std_logic_vector(17 downto 0);
      clk_to_xpoint_out_p: out std_logic;
      clk_to_xpoint_out_n: out std_logic;
      si5326_top_rst: out std_logic;
      si5326_top_int: in std_logic;
      si5326_top_lol: in std_logic;
      si5326_top_scl: out std_logic;
      si5326_top_sda: inout std_logic;
      si5326_bot_rst: out std_logic;
      si5326_bot_int: in std_logic;
      si5326_bot_lol: in std_logic;
      si5326_bot_scl: out std_logic;
      si5326_bot_sda: inout std_logic;
      si570_scl_out: out std_logic;
      si570_sda_out: out std_logic;
      si570_sda_in: in std_logic;
      minipod_top_rst_b: out std_logic;
      minipod_top_scl: out std_logic;
      minipod_top_sda_o: out std_logic;
      minipod_top_sda_i: in std_logic;
      minipod_bot_rst_b: out std_logic;
      minipod_bot_scl: out std_logic;
      minipod_bot_sda_o: out std_logic;
      minipod_bot_sda_i: in std_logic;
      mezz_p: out std_logic_vector(29 downto 0);
      mezz_n: out std_logic_vector(29 downto 0);
      refclkp: in std_logic_vector(N_REFCLK - 1 downto 0);
      refclkn: in std_logic_vector(N_REFCLK - 1 downto 0)
   );

end top;

architecture rtl of top is
```

```
   signal clk_ipb, rst_ipb, clk40ish, clk40, rst40, eth_refclk: std_logic;
   signal clk40_rst, clk40_sel, clk40_lock, clk40_stop, nuke: std_logic;
   signal soft_rst: std_logic;
   signal clk_p, rst_p: std_logic;
   signal clks_aux, rsts_aux: std_logic_vector(2 downto 0);

   signal si5326_top_sda_o, si5326_bot_sda_o, si570_sda_o: std_logic;

   signal ipb_in_ctrl, ipb_in_ttc, ipb_in_datapath: ipb_wbus;
   signal ipb_in_readout: ipb_wbus;
   signal ipb_in_payload, ipb_in_formatter, ipb_in_qdr: ipb_wbus;
   signal ipb_out_ctrl, ipb_out_ttc, ipb_out_datapath: ipb_wbus;
   signal ipb_out_readout: ipb_wbus;
   signal ipb_out_payload, ipb_out_formatter, ipb_out_qdr: ipb_rbus;

   signal payload_d, payload_q: ldata(N_REGION * 4 - 1 downto 0);
   signal qsel: std_logic_vector(7 downto 0);
   signal board_id: std_logic_vector(31 downto 0);
   signal ttc_l1a, ttc_l1a_dist, dist_lock, oc_flag, ec_flag: std_logic;
   signal payload_bc0, ttc_l1a_throttle, ttc_l1a_flag: std_logic;
   signal ttc_cmd, ttc_cmd_dist: ttc_cmd_t;
   signal bunch_ctr: bctr_t;
   signal evt_ctr, orb_ctr: eoctr_t;
   signal tmt_sync: tmt_sync_t;

   signal clkmon: std_logic_vector(2 downto 0);

   signal cap_bus: daq_cap_bus;
   signal daq_bus_top, daq_bus_bot: daq_bus;
   signal ctrs: ttc_stuff_array(N_REGION - 1 downto 0);
   signal rst_loc, clken_loc: std_logic_vector(N_REGION - 1 downto 0);
   signal mezz, mezz_en: std_logic_vector(29 downto 0);

begin

-- Clocks and control IO

   infra: entity work.mp7xe_infra
      port map(
         gt_clkp => eth_clkp,
         gt_clkn => eth_clkn,
         gt_txp => eth_txp,
         gt_txn => eth_txn,
         gt_rxp => eth_rxp,
         gt_rxn => eth_rxn,
         leds => leds,
         uc_pipe_nrd => ebi_nrd,
         uc_pipe_nwe => ebi_nwe,
         uc_pipe => ebi_d,
         uc_spi_miso => ebi_a(7),
         uc_spi_mosi => ebi_a(6),
```

```
      uc_spi_sck => ebi_a(5),
      uc_spi_cs_b => ebi_a(4),
      clk_ipb => clk_ipb,
      rst_ipb => rst_ipb,
      clk40ish => clk40ish,
      refclk_out => eth_refclk,
      nuke => nuke,
      soft_rst => soft_rst,
      oc_flag => oc_flag,
      ec_flag => ec_flag,
      clk_cntrl => clk_cntrl,
      si5326_top_rst => si5326_top_rst,
      si5326_top_int => si5326_top_int,
      si5326_top_lol => si5326_top_lol,
      si5326_top_scl => si5326_top_scl,
      si5326_top_sda_i => si5326_top_sda,
      si5326_top_sda_o => si5326_top_sda_o,
      si5326_bot_rst => si5326_bot_rst,
      si5326_bot_int => si5326_bot_int,
      si5326_bot_lol => si5326_bot_lol,
      si5326_bot_scl => si5326_bot_scl,
      si5326_bot_sda_i => si5326_bot_sda,
      si5326_bot_sda_o => si5326_bot_sda_o,
      si570_scl => si570_scl_out,
      si570_sda_i => si570_sda_in,
      si570_sda_o => si570_sda_out,
      minipod_top_rst_b => minipod_top_rst_b,
      minipod_top_scl => minipod_top_scl,
      minipod_top_sda_o => minipod_top_sda_o,
      minipod_top_sda_i => minipod_top_sda_i,
      minipod_bot_rst_b => minipod_bot_rst_b,
      minipod_bot_scl => minipod_bot_scl,
      minipod_bot_sda_o => minipod_bot_sda_o,
      minipod_bot_sda_i => minipod_bot_sda_i,
      ipb_in_ctrl => ipb_out_ctrl,
      ipb_out_ctrl => ipb_in_ctrl,
      ipb_in_ttc => ipb_out_ttc,
      ipb_out_ttc => ipb_in_ttc,
      ipb_in_datapath => ipb_out_datapath,
      ipb_out_datapath => ipb_in_datapath,
      ipb_in_readout => ipb_out_readout,
      ipb_out_readout => ipb_in_readout,
      ipb_in_payload => ipb_out_payload,
      ipb_out_payload => ipb_in_payload
    );

  si5326_top_sda <= '0' when si5326_top_sda_o = '0' else 'Z';
  si5326_bot_sda <= '0' when si5326_bot_sda_o = '0' else 'Z';

  ipb_out_qdr <= IPB_RBUS_NULL;
```

```
-- Control registers and board IO

   ctrl: entity work.mp7_ctrl
      port map(
         clk => clk_ipb,
         rst => rst_ipb,
         ipb_in => ipb_in_ctrl,
         ipb_out => ipb_out_ctrl,
         nuke => nuke,
         soft_rst => soft_rst,
         board_id => board_id,
         clk40_rst => clk40_rst,
         clk40_sel => clk40_sel,
         clk40_lock => clk40_lock,
         clk40_stop => clk40_stop
      );

-- TTC signal handling

   ttc: entity work.mp7_ttc
      port map(
         clk => clk_ipb,
         rst => rst_ipb,
         mmcm_rst => clk40_rst,
         sel => clk40_sel,
         lock => clk40_lock,
         stop => clk40_stop,
         ipb_in => ipb_in_ttc,
         ipb_out => ipb_out_ttc,
         clk40_in_p => clk40_in_p,
         clk40_in_n => clk40_in_n,
         clk40ish_in => clk40ish,
         clk40 => clk40,
         rst40 => rst40,
         clk_p => clk_p,
         rst_p => rst_p,
         clks_aux => clks_aux,
         rsts_aux => rsts_aux,
         ttc_in_p => ttc_in_p,
         ttc_in_n => ttc_in_n,
         ttc_cmd => ttc_cmd,
         ttc_cmd_dist => ttc_cmd_dist,
         ttc_l1a => ttc_l1a,
         ttc_l1a_flag => ttc_l1a_flag,
         ttc_l1a_dist => ttc_l1a_dist,
         l1a_throttle => ttc_l1a_throttle,
         dist_lock => dist_lock,
         bunch_ctr => bunch_ctr,
         evt_ctr => evt_ctr,
         orb_ctr => orb_ctr,
         oc_flag => oc_flag,
```

```
        ec_flag => ec_flag,
        tmt_sync => tmt_sync,
        monclk => clkmon
      );

-- MGTs, buffers and TTC fanout

   datapath: entity work.mp7_datapath
      port map(
        clk => clk_ipb,
        rst => rst_ipb,
        ipb_in => ipb_in_datapath,
        ipb_out => ipb_out_datapath,
        board_id => board_id,
        clk40 => clk40,
        clk_p => clk_p,
        rst_p => rst_p,
        ttc_cmd => ttc_cmd_dist,
        ttc_l1a => ttc_l1a_dist,
        lock => dist_lock,
        ctrs_out => ctrs,
        rst_out => rst_loc,
        clken_out => clken_loc,
        tmt_sync => tmt_sync,
        cap_bus => cap_bus,
        daq_bus_in => daq_bus_top,
        daq_bus_out => daq_bus_bot,
        payload_bc0 => payload_bc0,
        refclkp => refclkp,
        refclkn => refclkn,
        clkmon => clkmon,
        q => payload_d,
        d => payload_q
      );

-- Readout

   readout: entity work.mp7_readout
      port map(
        clk => clk_ipb,
        rst => rst_ipb,
        ipb_in => ipb_in_readout,
        ipb_out => ipb_out_readout,
        board_id => board_id,
        ttc_clk => clk40,
        ttc_rst => rst40,
        ttc_cmd => ttc_cmd,
        l1a => ttc_l1a,
        l1a_flag => ttc_l1a_flag,
        l1a_throttle => ttc_l1a_throttle,
        bunch_ctr => bunch_ctr,
```

```
        evt_ctr => evt_ctr,
        orb_ctr => orb_ctr,
        clk_p => clk_p,
        rst_p => rst_p,
        cap_bus => cap_bus,
        daq_bus_out => daq_bus_top,
        daq_bus_in => daq_bus_bot,
        amc13_refclk => eth_refclk
    );

-- Payload

    payload: entity work.mp7_payload
        port map(
        clk => clk_ipb,
        rst => rst_ipb,
        ipb_in => ipb_in_payload,
        ipb_out => ipb_out_payload,
        clk_payload => clks_aux,
        rst_payload => rsts_aux,
        clk_p => clk_p,
        rst_loc => rst_loc,
        clken_loc => clken_loc,
        ctrs => ctrs,
        bc0 => payload_bc0,
        d => payload_d,
        q => payload_q,
        gpio => mezz,
        gpio_en => mezz_en
    );

-- Debugging connector

    mezz_inst: entity work.mezz_out_lvds
        generic map(
        NMEZZ => mezz_p'length
    )
        port map(
        mezz => mezz,
        mezz_en => mezz_en,
        mezz_n => mezz_n,
        mezz_p => mezz_p
    );

-- Clock output

    clko: OBUFDS
        port map(
        I => '0',
        O => clk_to_xpoint_out_p,
        OB => clk_to_xpoint_out_n
```

```
    );

end rtl;
```

E.2 Algorithm top file

This file instantiates the BMTF algorithm. TF-algo-if instance interconnects all BMTF optical links the algorithm via d(0-35) and q(61).

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;

use work.ipbus.all;
use work.mp7_data_types.all;
use work.top_decl.all;
use work.mp7_brd_decl.all;
use work.mp7_ttc_decl.all;

entity mp7_payload is
   port(
      clk         : in std_logic;
      rst         : in std_logic;
      ipb_in      : in ipb_wbus;
      ipb_out     : out ipb_rbus;
      clk_payload : in std_logic_vector(2 downto 0);
      rst_payload : in std_logic_vector(2 downto 0);
      clk_p       : in std_logic;
      rst_loc     : in std_logic_vector(n_region-1 downto 0);
      clken_loc   : in std_logic_vector(n_region-1 downto 0);
      ctrs        : in ttc_stuff_array;
      bc0         : out std_logic;
      d           : in ldata(4*n_region-1 downto 0);
      q           : out ldata(4*n_region-1 downto 0);
      gpio        : out std_logic_vector(29 downto 0);
      gpio_en     : out std_logic_vector(29 downto 0)
   );

end mp7_payload;

architecture rtl of mp7_payload is

  signal tech_trigger : std_logic;

begin


  payload : entity work.TF_algo_if
    port map(
      d_n2w_osl    => d (4),
```

```
d_n2w_osh    => d (5),
d_n2w_lsl    => d (0),
d_n2w_lsh    => d (1),
d_n2w_rsl    => d (2),
d_n2w_rsh    => d (3),

d_n1w_osl    => d (12),
d_n1w_osh    => d (13),
d_n1w_lsl    => d (8),
d_n1w_lsh    => d (9),
d_n1w_rsl    => d (10),
d_n1w_rsh    => d (11),

d_0w_osl     => d (20),
d_0w_osh     => d (21),
d_0w_lsl     => d (16),
d_0w_lsh     => d (17),
d_0w_rsl     => d (18),
d_0w_rsh     => d (19),

d_p1w_osl    => d (22),
d_p1w_osh    => d (23),
d_p1w_lsl    => d (24),
d_p1w_lsh    => d (25),
d_p1w_rsl    => d (26),
d_p1w_rsh    => d (27),

d_p2w_osl    => d (28),
d_p2w_osh    => d (29),
d_p2w_lsl    => d (32),
d_p2w_lsh    => d (33),
d_p2w_rsl    => d (34),
d_p2w_rsh    => d (35),

clk240       => clk_p,
rst240       => '0',

q1_n2        => q (0),
q1_n1        => q (1),
q1_n0        => q (2),
q1_p0        => q (3),
q1_p1        => q (4),
q1_p2        => q (5),

q2_n2        => q (6),
q2_n1        => q (7),
q2_n0        => q (8),
q2_p0        => q (9),
q2_p1        => q (10),
q2_p2        => q (11),
```

```
    tr_n2        => q (12),
    tr_n1        => q (13),
    tr_n0        => q (14),
    tr_p0        => q (15),
    tr_p1        => q (16),
    tr_p2        => q (17),

    et_n2        => q (18),
    et_n1        => q (19),
    et_n0        => q (20),
    et_p0        => q (21),
    et_p1        => q (22),
    et_p2        => q (23),

    muon_output  => q (61),
    tech_trigger => tech_trigger,

    ipb_in       => ipb_in,
    ipb_out      => ipb_out,
    rst_ipb      => rst,
    ipb_clk      => clk,

    bc0          => bc0,
    clk40        => clk_payload(0),
    rst40        => rst_payload(0),
    clk_payload  => clk_payload(1),
    rst_payload  => rst_payload(1),
    clk_payload2 => clk_payload(2),
    rst_payload2 => rst_payload(2)
  );

  null_l_gen: for i in 60 downto 24 generate
  begin
    q(i).data <= (others=>'0');
    q(i).valid <= '1';
    q(i).start <= '0';
    q(i).strobe <= '1';
  end generate;

  null_h_gen: for i in 71 downto 62 generate
  begin
    q(i).data <= (others=>'0');
    q(i).valid <= '1';
    q(i).start <= '0';
    q(i).strobe <= '1';
  end generate;

  gpio    <= "00000000000000000000000000000000" & tech_trigger;
  gpio_en <= "00000000000000000000000000000001";

END rtl;
```

E.3 VHDL function designed to classify muons order used in the wedge sorter block of the BMTF

Wedge sorter block of BMTF chooses the best 3-muon candidates from the 12 that the track finders produce in the BMTF processor. The VHDL sorter block has been replaced because the initial was causing timing error after the design accelerated the processing time using 160-MHz algorithm clock. The new wedge sorter is based on a VHDL entity that implement the function shown below:

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.ALL;

package sorter_data_types is

   constant DATAI_WIDTH : integer := 13;
   constant DATAO_WIDTH : integer := 12;
   constant SORT_WIDTH : integer := 3;

   type sorter_data_in is array (natural range <>) of
      std_logic_vector(DATAI_WIDTH-1 downto 0);

   type sorter_data_out is array (natural range <>) of
      std_logic_vector(DATAO_WIDTH-1 downto 0);

   function SORT (VEC : sorter_data_in) return sorter_data_in;

end sorter_data_types;

package body sorter_data_types is

   function SORT (VEC : sorter_data_in) return sorter_data_in is
      type cnt_t is array (0 to VEC'HIGH) of integer range 0 to VEC'HIGH;
      variable cnt : cnt_t :=(others=>0);
      variable vec_v, vec_out : sorter_data_in(0 to VEC'HIGH);
   begin
      vec_v := VEC;
      for i in 0 to vec_v'HIGH-1 loop
         for j in i+1 to vec_v'HIGH loop
            if unsigned(vec_v(i)) <= unsigned(vec_v(j)) then
               cnt(i) := cnt(i) + 1;
            else
               cnt(j) := cnt(j) + 1;
            end if;
         end loop;
      end loop;
      for t in 0 to vec_v'HIGH loop
         vec_out(t) := std_logic_vector(to_unsigned(cnt(t),DATAI_WIDTH));
```

```
      end loop;
      return vec_out;
   end function;

end sorter_data_types;
```

The function **sort** is called in the $sorter_proc$ process of the sorter entity. The output of the sorter block ranks the 12-muon candidates and acts as input of a multiplexer which defines the 3 best-muon candidates to the output of the BMTF processor.

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;
use work.sorter_data_types.all;

entity sorter is
   generic(num_in : integer :=12;
        num_out : integer :=3
      );
    port(clk : in std_logic;
       din  : in sorter_data_in(0 to num_in-1);
       dout : out sorter_data_out(0 to num_out-1)
   );
end sorter;

architecture behavioral of sorter is
   signal din_s : sorter_data_in(0 to num_in-1);
   signal sort_s : sorter_data_in(0 to num_in-1);
begin

   din_s <= din;

   sorter_proc: process(clk,din_s)
   begin
      if rising_edge(clk) then
         sort_s <= sort(din_s);
      end if;
   end process;

   out_proc: process(sort_s)
   begin
      if     sort_s(0) = "0000000000000" then dout(0) <= "000000000001";
      elsif  sort_s(1) = "0000000000000" then dout(0) <= "000000000010";
      elsif  sort_s(2) = "0000000000000" then dout(0) <= "000000000100";
      elsif  sort_s(3) = "0000000000000" then dout(0) <= "000000001000";
      elsif  sort_s(4) = "0000000000000" then dout(0) <= "000000010000";
      elsif  sort_s(5) = "0000000000000" then dout(0) <= "000000100000";
      elsif  sort_s(6) = "0000000000000" then dout(0) <= "000001000000";
      elsif  sort_s(7) = "0000000000000" then dout(0) <= "000010000000";
```

```
    elsif sort_s(8) = "0000000000000" then dout(0) <= "000100000000";
    elsif sort_s(9) = "0000000000000" then dout(0) <= "001000000000";
    elsif sort_s(10)= "0000000000000" then dout(0) <= "010000000000";
    elsif sort_s(11)= "0000000000000" then dout(0) <= "100000000000";
    else                                   dout(0) <= "000000000000";
    end if;
    if    sort_s(0) = "0000000000001" then dout(1) <= "000000000001";
    elsif sort_s(1) = "0000000000001" then dout(1) <= "000000000010";
    elsif sort_s(2) = "0000000000001" then dout(1) <= "000000000100";
    elsif sort_s(3) = "0000000000001" then dout(1) <= "000000001000";
    elsif sort_s(4) = "0000000000001" then dout(1) <= "000000010000";
    elsif sort_s(5) = "0000000000001" then dout(1) <= "000000100000";
    elsif sort_s(6) = "0000000000001" then dout(1) <= "000001000000";
    elsif sort_s(7) = "0000000000001" then dout(1) <= "000010000000";
    elsif sort_s(8) = "0000000000001" then dout(1) <= "000100000000";
    elsif sort_s(9) = "0000000000001" then dout(1) <= "001000000000";
    elsif sort_s(10)= "0000000000001" then dout(1) <= "010000000000";
    elsif sort_s(11)= "0000000000001" then dout(1) <= "100000000000";
    else                                   dout(1) <= "000000000000";
    end if;
    if    sort_s(0) = "0000000000010" then dout(2) <= "000000000001";
    elsif sort_s(1) = "0000000000010" then dout(2) <= "000000000010";
    elsif sort_s(2) = "0000000000010" then dout(2) <= "000000000100";
    elsif sort_s(3) = "0000000000010" then dout(2) <= "000000001000";
    elsif sort_s(4) = "0000000000010" then dout(2) <= "000000010000";
    elsif sort_s(5) = "0000000000010" then dout(2) <= "000000100000";
    elsif sort_s(6) = "0000000000010" then dout(2) <= "000001000000";
    elsif sort_s(7) = "0000000000010" then dout(2) <= "000010000000";
    elsif sort_s(8) = "0000000000010" then dout(2) <= "000100000000";
    elsif sort_s(9) = "0000000000010" then dout(2) <= "001000000000";
    elsif sort_s(10)= "0000000000010" then dout(2) <= "010000000000";
    elsif sort_s(11)= "0000000000010" then dout(2) <= "100000000000";
    else                                   dout(2) <= "000000000000";
    end if;
  end process;

end behavioral;
```

Appendix F

Validation of 10-Gb/s asynchonous links implemented for KC705 and VC707 development boards

As described in Section 4.4.1.1, the asynchronous protocol is based on the widely used 10-Gb/s link running with 8b10b encoding [59]. The asynchronous protocol injects one additional k (idle) character every 25 data frames in the transmitter side. This character is rejected in the receiver side, and therefore it reduces the 10-Gb/s link throughput to 9.6 Gb/s (Figure F.1).

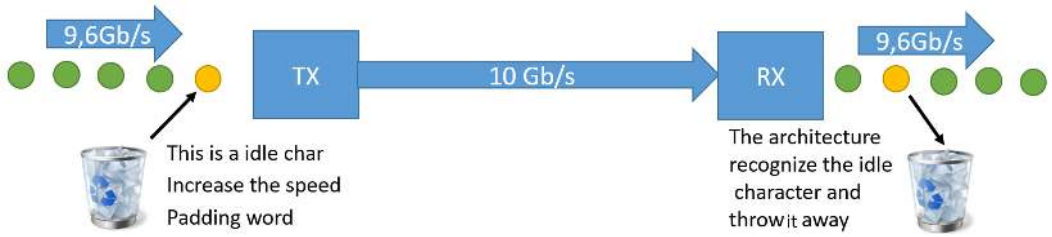


Figure F.1: 9.6-Gb/s asynchronous link

This additional idle character assures a stable link running free of alignment losses due to clock phase uncertainties of the LHC clock. The FPGA transceivers are very sensitive to the jitter and the phase change of the "reference" clock that drives them. Synchronous links use a common reference clock source from the LHC collider. They are affected by any phase change that often occurs in the LHC clock. On the contrary the asynchronous links use differed oscillator clock sources as reference clocks, locally on each trigger board while they also receive the LHC clock as a second clock. The data frames pass through the two clock domains (transition and algorithm) using the 0x000504bc idle character. This technique keeps the link stable as well as ensures a secure crossing over the data domains. A basic diagram of the asynchronous protocol is shown in Figure F.2. The blocks are divided into two parts by the black dashed line. On the left side, the logic of the transmitter is shown and on the right side appears the logic of the receiver. The algorithm of the transmitter (TX ALGO) forward its results to the TX Elastic FIFO (First In - First Out) block using a bus of 192-bits. This bus runs in 40 MHz and a serializer converts it to 32-bit frames running at 240 MHz. Then the elastic FIFO logic writes the 32-bit frames to

a 250-MHz domain using a *valid flag* that indicates the frame number to be forward for the 24 frames of the 240-MHz domain to the 25 frames 250-MHz domain.

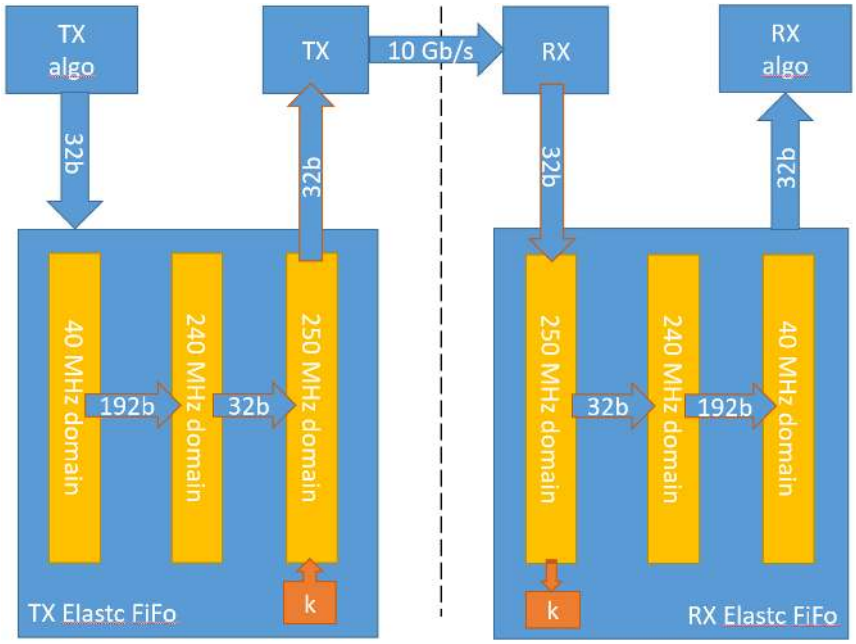


Figure F.2: Block diagram of the asynchronous protocol 10 Gb/s

The logic injects the additional k frame (idle character) of the 250-MHz domain. The data are forward to the TX block that instantiates a transceiver and use a 10-Gb/s serial protocol with 8b10b encoding. On the receiver side the data stream is captured and aligned. The data are formed to a 32-bit data frames running at 250 MHz. Except from the k characters of the 8b10b decoding the additional k frames of the asynchronous protocol are recognized and detected. The valid frames are captured in the 240-MHz block domain. A deserializer converts the 32-bit bus to a 192-bit bus running at 40 MHz which is used in the receiver algorithm.

F.1 Simulation results

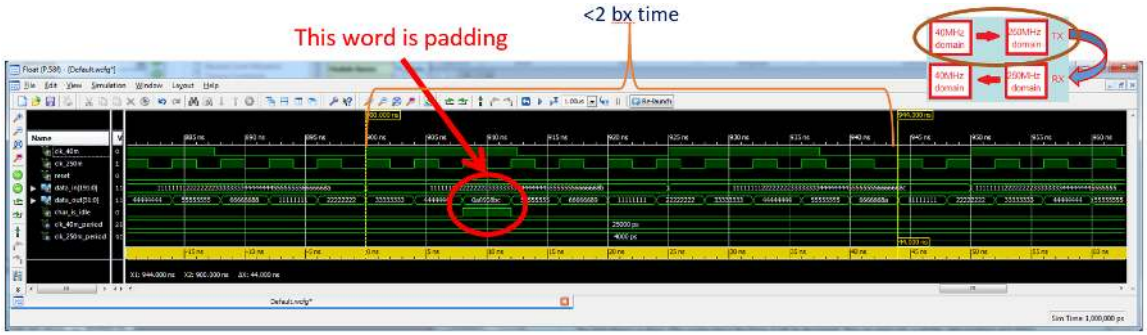


Figure F.3: TX Elastic FIFO of the asynchronous protocol 10 Gb/s, output of ISim Xilinx software [79].

Figure F.3 illustrates the results of the behavioral simulation of the TX Elastic FIFO. As is shown the 192-bits of the 40-MHz domain have been successfully

converted to 6 x 32-bit frames in the 250-MHz domain. The idle words are injected to the 250-MHz domain bus in order to increase the throughput to 10 Gb/s. The latency of the TX Elastic FIFO is less than 2 bunch crossings.

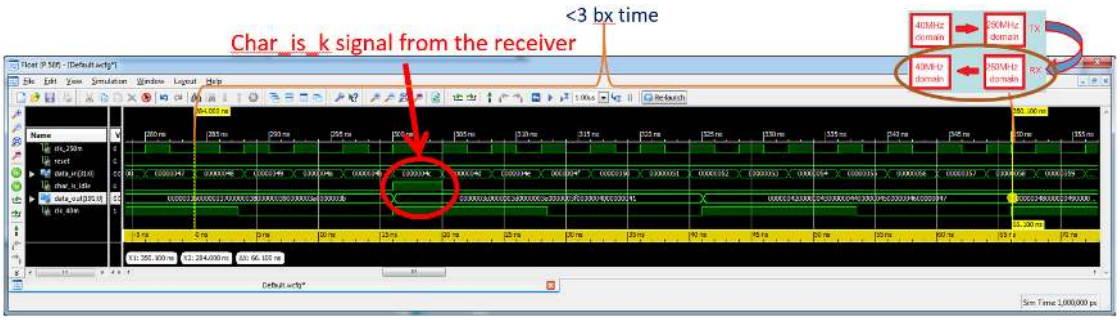


Figure F.4: RX Elastic FIFO of the asynchronous protocol 10 Gb/s, output of ISim Xilinx software [79].

Figure F.4 illustrates the stimulus of the RX Elastic FIFO. As shown the data of the 250 MHz have been converted correctly to the 40-MHz domain with a latency less than 3 bunch crossings. The k character is masked in red cycle.

F.2 Setup

The asynchronous 10-Gb/s protocol has been tested in HEPLAB laboratory in the University of Ioannina using KC705 (Kintex7) and VC707 (Virtex7) evaluation boards. VHDL blocks of RX and TX Elastic FIFOs (simulated above) are implemented to both Kintex7 (*XC7K325T-2FFG900*) and Virtex7 (*XC7VX485-2FFG1761*) FPGAs. The firmware preforms the same 10-Gb/s serial protocol with 8b10b encoding in the two systems. As shown in the Figure F.5, KC705 and VC707 boards are interconnected with a common optical fiber and receive a clock that represents the LHC clock. Both systems rise a flag that indicates the presence of the idle character. The frag drives an electrical signal that is illustrated to the oscilloscope. The oscilloscope is used in order to measure the latency of the data transaction.

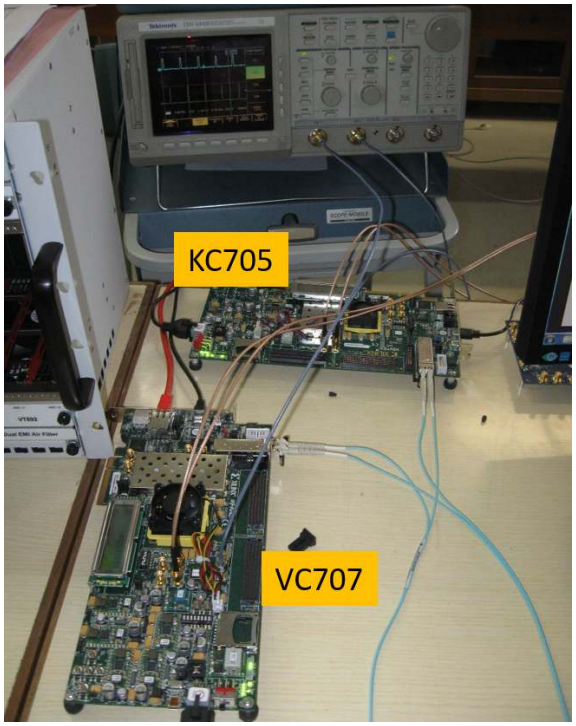


Figure F.5: Testing the asynchronous protocol using KC705 and VC707 cards

Both cards are equipped with a jitter cleaner module (SI5324, Silicon labs) to drive the transceivers. This module is configurable through an I^2C channel switch (PCA9548, Texas Instruments). The jitter attenuator has over than 100 registers that define the needed parameters in order to minimize the clock jitter. The required

register values are calculated by a dedicated software (*DSPLLsim*) from Silicon Labs [80]. Then a bash script writes the addresses, the values and the number of the registers to be written to a VHDL package. The design uses a two transactions of the I^2C interface to enable the Si5324 path of the PCA9548 switch and to perform multiple writes to the Si5324 registers.

F.3 Validation

Figure F.6 shows the chipscope tool used to validate the asynchronous 10-Gb/s protocol. The testbench includes two virtual I/O (VIO) windows (upper left) with which the user resets the system, configures the jitter attenuator, configures the transceivers, starts the word generators and the word checker and setup the delay used by the frame checker in order to compare the received frames with those generated by the frame generator.

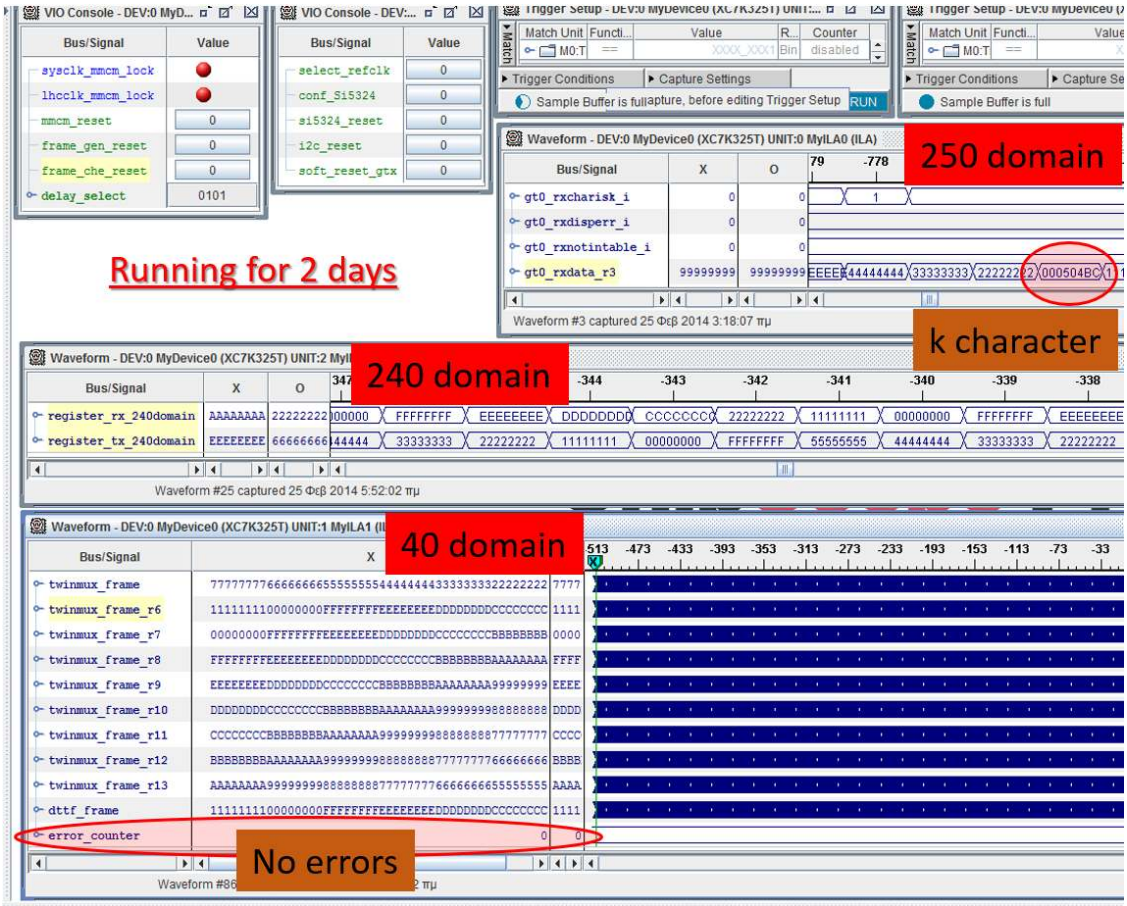


Figure F.6: Validation of the 10-Gb/s asynchronous protocol, output of Chipscope Xilinx software [81].

The VC707 is sending serial data to the KC705. Both have implemented the TX and RX Elastic FIFOs as presented in Figure F.2. The three clock domains of the RX Elastic FIFOs are presented in the Figure F.6. As shown in the *gt0_rxdata_r3* bus of 250-MHz clock domain the deserialized k character "000504BC" interrupts the valid data "22222222" → "11111111" sequence. In the 240-MHz clock domain the k character is skipped and the sequence is not interrupted (bus *register_rx_240domain*).

In the 40-MHz clock domain the 32-bit frames have been successfully transformed to 192-bit words.

The demonstrator uses one 192-bit word generator and a 192-bit word checker on each FPGA. In the receiver part the *error_counter* bus counts the mismatches between received 192-bit bus of the 40-MHz domain and the delayed words of the word generator logic. The delay is determined by the user with the *delay_select* which in this case is "0101" and indicates 5 bunch crossings delay for the total chain: KC705 192-bit word generator → KC705 32 bits @ 240 MHz → KC705 32 bits @ 250 MHz → fiber length → VC707 32 bit @ 250 MHz → VC707 32 bits @ 240 MHz → VC707 192-bit word checker.

As shown in Figure F.6 the test was running continuously for 2 days error free, validating the 10-Gb/s asynchronous protocol used in the Barrel Muon Track Finder.

Bibliography

[1] A Tapper and Darin Acosta. CMS Technical Design Report for the Level-1 Trigger Upgrade. Technical Report CERN-LHCC-2013-011. CMS-TDR-12, CERN, Geneva, Jun 2013. Additional contacts: Jeffrey Spalding, Fermilab, Jeffrey.Spalding@cern.ch Didier Contardo, Universite Claude Bernard-Lyon I, didier.claude.contardo@cern.ch.

[2] J. Ero, I. Evangelou, G. Flouris, C. Foudas, L. Guiducci, N. Loukas, N. Manthos, I. Papadopoulos, E. Paradas, S. Sotiropoulos, P. Sphicas, A. Triossi, and C. Wulz. The cms level-1 trigger barrel track finder. *Journal of Instrumentation*, 11(03):C03038, 2016.

[3] A. Triossi, M. Bellato, J.M. Cela Ruiz, J. Ero, C. Fernandez Bedoya, G. Flouris, C. Foudas, L. Guiducci, N. Loukas, A. Navarro Tobar, S. Mallios, G. Masetti, F. Montecassiano, E. Paradas, I. Redondo Fernandez, D. Redondo Ferrero, J. Sastre, P. Sphicas, S. Ventura, and C. Wulz. The cms barrel muon trigger upgrade. *Journal of Instrumentation*, 12(01):C01095, 2017.

[4] Dinyar Rabady, Janos Ero, Giannis Flouris, Jonathan Fulcher, Nikitas Loukas, Evangelos Paradas, Thomas Reis, Hannes Sakulin, and Claudia-Elisabeth Wulz. Upgrade of the {CMS} muon trigger system in the barrel region. *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, pages –, 2016.

[5] Dinyar Rabady, Janos Ero, Giannis Flouris, Jonathan Fulcher, Nikitas Loukas, Evangelos Paradas, Thomas Reis, Hannes Sakulin, and Claudia-Elisabeth Wulz. Upgrade of the CMS muon trigger system in the barrel region. *Nucl. Instrum. Meth.*, A845:616–620, 2017.

[6] N.Loukas et al. Detector Note - Interface and notes between the TwinMux and Barrel Muon Track Finder in the Upgraded CMS Trigger for 2016. Technical Report DN-16-008, CERN, Geneva, Sept 2016.

[7] N.Loukas. BMTF Collaboration. https://twiki.cern.ch/twiki/bin/viewauth/CMS/BMTF.

[8] Georges Aad et al. Observation of a new particle in the search for the Standard Model Higgs boson with the ATLAS detector at the LHC. *Phys. Lett.*, B716:1–29, 2012.

[9] Serguei Chatrchyan et al. Observation of a new boson at a mass of 125 GeV with the CMS experiment at the LHC. *Phys. Lett.*, B716:30–61, 2012.

[10] Lyndon R Evans. *The large hadron collider: a marvel of technology*. EPFL Press, 2009.

[11] S. Chatrchyan et al. The CMS experiment at the CERN LHC. *JINST*, 3:S08004, 2008.

[12] A. Hervé et al. Status of the construction of the CMS magnet. *IEEE Trans. Appl. Supercond.*, 14(2):542–547, 2004.

[13] V Karimäki, M Mannelli, P Siegrist, H Breuker, A Caner, R Castaldi, K Freudenreich, G Hall, R Horisberger, M Huhtinen, and A Cattai. *The CMS tracker system project: Technical Design Report*. Technical Design Report CMS. CERN, Geneva, 1997.

[14] Rong-Shyang Lu. The Phase 1 Upgrade of the CMS Pixel Detector. *PoS*, Vertex2012:036, 2013.

[15] A Dominguez, D Abbaneo, K Arndt, N Bacchetta, A Ball, E Bartz, W Bertl, G M Bilei, G Bolla, H W K Cheung, M Chertok, S Costa, N Demaria, Daniel Dominguez Vazquez, K Ecklund, W Erdmann, K Gill, G Hall, K Harder, F Hartmann, R Horisberger, W Johns, H C Kaestli, K Klein, D Kotlinski, S Kwan, M Pesaresi, H Postema, T Rohe, C Schäfer, A Starodumov, S Streuli, A Tricomi, P Tropea, J Troska, F Vasey, and W Zeuner. CMS Technical Design Report for the Pixel Detector Upgrade. Technical Report CERN-LHCC-2012-016. CMS-TDR-11, CERN, Geneva, Sep 2012. Additional contacts: Jeffrey Spalding, Fermilab, Jeffrey.Spalding@cern.ch Didier Contardo, Universite Claude Bernard-Lyon I, didier.claude.contardo@cern.ch.

[16] Paolo Azzurri. The cms silicon strip tracker. *Journal of Physics: Conference Series*, 41(1):127, 2006.

[17] A Benaglia. The cms ecal performance with examples. *Journal of Instrumentation*, 9(02):C02008, 2014.

[18] J Mans, J Anderson, B Dahmes, P de Barbaro, J Freeman, T Grassi, E Hazen, J Mans, R Ruchti, I Schimdt, T Shaw, C Tully, J Whitmore, and T Yetkin. CMS Technical Design Report for the Phase 1 Upgrade of the Hadron Calorimeter. Technical Report CERN-LHCC-2012-015. CMS-TDR-10, CERN, Geneva, Sep 2012. Additional contact persons: Jeffrey Spalding, Fermilab, spalding@cern.ch, Didier Contardo, Universite Claude Bernard-Lyon I, contardo@cern.ch.

[19] Kerem Cankocak, Yasar Onel, Pawel de Barbaro, and Dima Vishnevskiy. CMS HCAL Installation and Commissioning. Technical Report CMS-CR-2008-047, CERN, Geneva, Jul 2008.

[20] *The CMS muon project: Technical Design Report*. Technical Design Report CMS. CERN, Geneva, 1997.

[21] S Chatrchyan et al. Performance of the CMS Drift Tube Chambers with Cosmic Rays. *JINST*, 5:T03015, 2010.

[22] R Travaglini. Local Trigger Electronics for the CMS Drift Tubes Muon detector. Technical Report CMS-CR-2004-005, CERN, Geneva, Feb 2004.

[23] A Colaleo, A Safonov, A Sharma, and M Tytgat. CMS Technical Design Report for the Muon Endcap GEM Upgrade. Technical Report CERN-LHCC-2015-012. CMS-TDR-013, Jun 2015.

[24] CMS Collaboration. Performance of the cms drift-tube chamber local trigger with cosmic rays. *Journal of Instrumentation*, 5(03):T03003, 2010.

[25] *Advanced TCA base specification: advanced TCA*. PICMG, Wakefield, MA, 2008. The document can be consulted by contacting: PH-ESE : Markus Joos or Evelyne Dho.

[26] G Bauer, T Bawej, U Behrens, J Branson, O Chaze, S Cittolin, J A Coarasa, G L Darlea, C Deldicque, M Dobson, A Dupont, S Erhan, D Gigi, F Glege, G Gomez-Ceballos, R Gomez-Reino, C Hartl, J Hegeman, A Holzner, L Masetti, F Meijers, E Meschi, R K Mommsen, S Morovic, C Nunez-Barranco-Fernandez, V O'Dell, L Orsini, W Ozga, C Paus, A Petrucci, M Pieri, A Racz, O Raginel, H Sakulin, M Sani, C Schwick, A C Spataru, B Stieger, K Sumorok, J Veverka, C C Wakefield, and P Zejdl. 10 gbps tcp/ip streams from the fpga for the cms daq eventbuilder network. *Journal of Instrumentation*, 8(12):C12039, 2013.

[27] S. Dasu et al. CMS. The TriDAS project. Technical design report, vol. 1: The trigger systems. 2000.

[28] Andrew Rose. A Grand Unified Trigger for CMS. Sep 2011.

[29] B. Kreis et al. Run 2 Upgrades to the CMS Level-1 Calorimeter Trigger. *JINST*, 11(01):C01051, 2016.

[30] Pamela Renee Klabbers. Operation and Performance of the Upgraded CMS Calorimeter Trigger in LHC Run 2. Technical Report CMS-CR-2015-317, CERN, Geneva, Nov 2015.

[31] M Baber, M Blake, J Brooke, M Cepeda Hermida, S Dasu, T Durkin, S Fayer, E K Friis, T Gorski, G Hall, K Harder, G Iles, S Ives, J Jones, P R Klabbers, A G Levine, C Lucas, R Lucas, D Newbold, J Marrouche, S Paramesvaran, T M Perry, A Rose, D Sankey, W Smith, A Tapper, A Thea, and T Williams. Development and testing of an upgrade to the cms level-1 calorimeter trigger. *Journal of Instrumentation*, 9(01):C01006, 2014.

[32] G. Iles, J. Jones, and A. Rose. Experience powering Xilinx Virtex-7 FPGAs. *JINST*, 8:C12037, 2013.

[33] G. Hall, D. Newbol, M. Pesaresi, and A. Rose. A time-multiplexed track-trigger architecture for cms. *Journal of Instrumentation*, 9(10):C10034, 2014.

[34] Andrew Rose. A Combined Conventional and Time-multiplexed Calorimeter Trigger for CMS. Oct 2011.

[35] K. Compton et al. The MP7 and CTP-6: Multi-hundred Gbps processing boards for calorimeter trigger upgrades at CMS. *JINST*, 7:C12024, 2012.

[36] Andrea Triossi, Marco Bellato, Roberto Isocrate, Fabio Montecassiano, and Sandro Ventura. A New Data Concentrator for the CMS Muon Barrel Track Finder. *PoS*, TIPP2014:412, 2014.

[37] AVAGO Technologies. Twelve-channel transmitter and receiver pluggable. http://www.mouser.com/ds/2/38/AV02-1479EN_DS_AFBR-776xxZ_29Jan2013-271926.pdf.

[38] Chun-Jie Wang, Zhen-An Liu, Jing-Zhou Zhao, and Zhao Liu. Design of a high throughput electronics module for high energy physics experiments. *Chinese Physics C*, 40(6):066102, 2016.

[39] D. Acosta et al. The CMS Modular Track Finder boards, MTF6 and MTF7. *JINST*, 8:C12034, 2013.

[40] Wojciech Zabolotny and Adrian Pawel Byszuk. Algorithm and implementation of muon trigger and data transmission system for barrel-endcap overlap region of the CMS detector. Technical Report CMS-CR-2015-261, CERN, Geneva, Oct 2015.

[41] Wojciech M. Zabołotny et al. FPGA implementation of overlap MTF trigger: preliminary study. *Proc. SPIE Int. Soc. Opt. Eng.*, 9290:929025, 2014.

[42] Vadateh. MCH UTC002 datasheet. http://www.vadatech.com/media/UTC002_UTC002_Datasheet.pdf.

[43] J. Wittmann, B. Arnold, H. Bergauer, M. Jeitler, T. Matsushita, D. Rabady, B. Rahbaran, and C.-E. Wulz. The upgrade of the cms global trigger. *Journal of Instrumentation*, 11(02):C02029, 2016.

[44] Vadateh. AMC502 datasheet. http://www.vadatech.com/media/AMC502_AMC502_Datasheet.pdf.

[45] B Rahbaran, B Arnold, H Bergauer, M Eichberger, and D Rabady. Microtca-based global trigger upgrade project for the cms experiment at lhc. *Journal of Instrumentation*, 6(12):C12054, 2011.

[46] Takashi Matsushita and Bernhard Arnold. Software for implementing trigger algorithms on the upgraded cms global trigger system. *Journal of Physics: Conference Series*, 664(8):082031, 2015.

[47] Daniele Trocino. The cms high level trigger. *Journal of Physics: Conference Series*, 513(1):012036, 2014.

[48] P. Sphicas. CMS: The TriDAS project. Technical design report, Vol. 2: Data acquisition and high-level trigger. 2002.

[49] Ignacio Jiménez Alfaro. *Beam Test of the Drift Tube Track Finder Muon Trigger at CMS*. PhD thesis, Madrid, Autonoma U., 2006.

[50] M Di Cosmo, V Bobillier, S Haas, M Joos, S Mico, F Vasey, and P Vichoudis. Evaluation results of xtca equipment for hep experiments at cern. *Journal of Instrumentation*, 8(12):C12015, 2013.

[51] M Di Cosmo, V Bobillier, S Haas, M Joos, S Mico, and F Vasey. Microtca and advancedtca equipment evaluation and customization for lhc experiments. *Journal of Instrumentation*, 10(01):C01008, 2015.

[52] Pentair. MicroTCA.4 datasheet. http://schroff.pentair.com/wcsstore/ExtendedSitesCatalogAssetStore/Attachment/SchroffAttachments/Documents/8_3_MicroTCA_e.pdf.

[53] NAT. Nat-power module. http://www.nateurope.com/products/NAT-PM-DC840.html.

[54] NAT. Nat-mch. http://www.nateurope.com/products/NAT-MCH.html.

[55] E. Hazen, A. Heister, C. Hill, J. Rohlf, S. X. Wu, and D. Zou. The AMC13XG: a new generation clock/timing/DAQ module for CMS MicroTCA. *JINST*, 8:C12036, 2013.

[56] Jeroen Guido Hegeman, Jean-marc Olivier Andre, Ulf Behrens, James Branson, Olivier Chaze, Sergio Cittolin, Georgiana Lavinia Darlea, Christian Deldicque, Zeynep Demiragli, Marc Dobson, Samim Erhan, Jonathan Richard Fulcher, Dominique Gigi, Frank Glege, Guillelmo Gomez Ceballos, Magnus Hansen, Andre Georg Holzner, Raul Jimenez Estupinan, Lorenzo Masetti, Franciscus Meijers, Emilio Meschi, Remigius Mommsen, Srecko Morovic, Vivian O'Dell, Luciano Orsini, Christoph Maria Ernst Paus, Marco Pieri, Attila Racz, Hannes Sakulin, Christoph Schwick, Dainius Simelevicius, Jan Troska, Paschalis Vichoudis, and Petr Zejdl. The CMS Timing Control and Distribution System. Technical Report CMS-CR-2015-321, CERN, Geneva, Dec 2015.

[57] Imperial College London. Mp7 user guide. http://www.hep.ph.ic.ac.uk/mp7/documents/UserGuideForTheMP7.latest.pdf.

[58] J. Hegeman. DAQ. Apr 2013.

[59] A.X. Widmer. 8b/10b encoding and decoding for high speed applications, December 20 2005. US Patent 6,977,599.

[60] Xilinx. 7 series transceivers. https://www.xilinx.com/support/documentation/user_guides/ug476_7Series_Transceivers.pdf.

[61] J.Lingemann et al. Detector Note - Interface between the Muon Track Finders and the micro-Global Muon Trigger in the Upgraded CMS Trigger for 2016. Technical Report DN-15-017, CERN, Geneva, Sept 2016.

[62] Measuring Electron Efficiencies at CMS with Early Data. 2008.

[63] Level-1 muon trigger performance in 2017 data and comparison with the legacy muon trigger system. Sep 2017.

[64] CMS collaboration. Level-1 trigger muon performance 2017 and legacy.

[65] Simone Bologna, Giuseppe Codispoti, Glenn Dirkx, Lukasz Kreczko, Christos Lazaridis, Evangelos Paradas, A Rose, Alessandro Thea, and Thomas Stephen Williams. SWATCH Common software for controlling and monitoring the

upgraded CMS Level-1 trigger. Technical Report CMS-CR-2016-121, CERN, Geneva, Jun 2016.

[66] H. Reithler. Cms dt type naming. https://web.physik.rwth-aachen.de/~reithler/050912DT_type_naming.pdf, 2005.

[67] Federico De Guio. The CMS data quality monitoring software: experience and future prospects. *J. Phys. Conf. Ser.*, 513:032024, 2014.

[68] Xilinx KC705 Evaluation. Ug810 - user guide. http://www.xilinx.com/support/documentation/boards_and_kits/kc705/ug810_KC705_Eval_Bd.pdf, 2016.

[69] Xilinx VC707 Evaluation. Ug885 - user guide. http://www.xilinx.com/support/documentation/boards_and_kits/vc707/ug885_VC707_Eval_Bd.pdf, 2016.

[70] M. Pesaresi, M. Barros Marin, G. Hall, M. Hansen, G. Iles, A. Rose, F. Vasey, and P. Vichoudis. The fc7 amc for generic daq & control applications in cms. *Journal of Instrumentation*, 10(03):C03036, 2015.

[71] PICMG. "mtca.0 r1.0 specifications". http://www.picmg.org/openstandards/microtca/, 2016.

[72] ANSI/VITA. "fmc specifications". http://www.vita.com/, 2016.

[73] N. Loukas. Results of the tcds fmc serial link tests. https://indico.cern.ch/event/300026/contributions/687597/attachments/565132/778584/Results_of_the_TCDS_FMC_serial_link_tests.pdf, 2013.

[74] Faster Technology. "fmc cards". http://www.fastertechnology.com/products/fmc/fm-s18.html, 2013.

[75] Jim Brooke, Karol Bunkowski, Ivan Cali, Carlos Ghabrous Larrea, Christos Lazaridis, and Alessandro Thea. SWATCH: common control SW for the uTCA-based upgraded CMS L1 Trigger. *J. Phys.: Conf. Ser.*, 664(8):082012. 8 p, 2015.

[76] C. Ghabrous Larrea, K. Harder, D. Newbold, D. Sankey, A. Rose, A. Thea, and T. Williams. Ipbus: a flexible ethernet-based control system for xtca hardware. *Journal of Instrumentation*, 10(02):C02019, 2015.

[77] MP7 software. Mp7 software news web page. https://twiki.cern.ch/twiki/bin/view/CMS/MP7SoftwareNews.

[78] N.Loukas. BMTF cactus trunk. https://svnweb.cern.ch/trac/cactus/browser/trunk/cactusupgrades/projects/bmtf.

[79] Xilinx. "ise simulator". https://www.xilinx.com/products/design-tools/isim.html.

[80] Silicon Labs. Dspllsim software. https://www.silabs.com/products/development-tools/software/clock.

[81] Xilinx. ‘ise chipscope pro ila. https://www.xilinx.com/support/documentation/sw_manuals/xilinx14_3/ug750.pdf.